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Schottky Characteristics and Interfacial Defects in Tungsten Silicide/GaAs and Palladium/GaAs Systems

T. Makimoto, M. Taniguchi*, K. Ogiwara**, T. Ikoma
Institute of Industrial Science, University of Tokyo
7-22-1, Roppongi, Minatoku, Tokyo 106
and
T. Okumura
Tokyo Metropolitan Unversity
2-1-1, Fukazawa, Setagayaku, Tokyo 158

Schottky characteristics and interfacial defects were investigeted in WSi/GaAs and Pd/GaAs systems. In as-deposited WSi/GaAs systems, no "EL2" signal was found but a new sputtering-induced defect ("ED5") was detected near the interface. After annealing, "EL2" appeared and "ED5" disappeared. The disappearance of "ED5" was correlated with improvement of the ideality factor. In Pd/GaAs systems, change of "EL2" density and the broadening of "EL2" spectrum is noticeable as compared with the Au/GaAs system. We propose a hypothetical model, that reaction of Pd with GaAs may extract excess arsenic atoms near the interface and reduce the concentration of "EL2".

1. Introduction

Metal-silicides play an important role in the present LSIs. Equivalent materials to silicides for GaAs are worthy of studying as future materials of GaAs LSIs. W-silicide is used as a gate metal for GaAs MESFETs.[1] The advantage is its resistance for high temperature treatment. Another material is a Pt/GaAs reaction layer which is also used as a gate metal.[2] The advantage lies in the fact that the depth of reaction layer can be controlled by the time of heat treatment, which allows the fine control of the threshold voltage in an MESFET. A system similar to Pt/GaAs is Pd/GaAs.[3] In this system, reaction proceeds at very low temperatures, being contrasted to a W-silicide/GaAs system.

It is important and interesting to study interfacial defects in W-silicide/GaAs and Pd/GaAs systems and their effects on Schottky characteristics. The object of this paper is to investigate correlation between interfacial defects and Schottky characteristics in these systems. Annealing behavior of deep levels in GaAs is also studied, since a W-silicide can stand high temperature treatment.

2. W-silicide/GaAs system

Sample and Measurement

Si and W were co-sputtered onto GaAs wafers at substrate temperature of 120 °C, input power of 80 W in Ar atmosphere of 4×10^{-2} Torr. The change of Schottky characteristics was minimized at Si composition ranging from 0.12 to 0.18 in the area ratio of sputtering target surface. Both non-doped n-type horizontal Bridgmann (HB) and liquid-encapsulated Czochralski(LEC) GaAs crystals were used. However, Schottky diodes formed on LEC GaAs showed poor voltage-current characteristics, and therefore only the results with HB GaAs are presented.

The barrier height ϕ and the ideality factor n were determined from voltage-current characteristic. Deep levels were measured by DLTS.

Schottky Characteristics

Schottky characteristic is represented by ϕ and n. The changes of ϕ and n with annealing are shown in Fig. 1. The annealing time was 15 min. and the annealing atmosphere was Ar. The as-deposited sample showed larger n and smaller ϕ. They were improved by annealing up to 600 °C.

* present address; Japan Mining Company Ltd.
** Student from Shibaura Institute of Technology

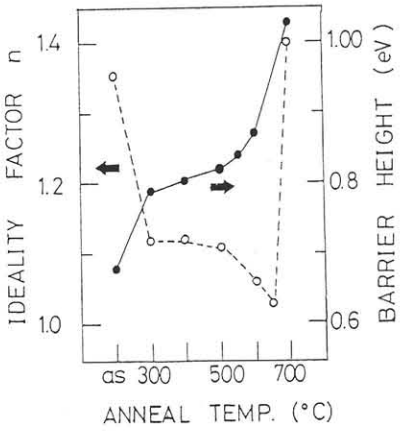

Fig. 1. Variation of Schottky barrier height (ϕ) and ideality factor(n) with annealing temperature determined by I-V characteristics at room temperature.

Deep Levels

Typical DLTS spectra are shown in Fig. 2. Two remarkable features were found. First, no "EL2" signal was observed in the as-deposited sample and appeared after annealing at 500 °C. The peak temperature shifted to lower temperature with annealing at higher temperatures up to 700 °C (not shown in the figure). Second, a new defect level which has activation energy of 0.52 eV and capture cross section of $3\times10^{-15}cm^2$, appeared in the as-deposited sample. This defect was localized very near the interface and annealed out at 300 °C. In addition to those levels, five deep levels were observed in this particular HB GaAs. The level ET7 appeared after 500 °C annealing. This is contrasted to another HB GaAs sample which contained ET7 as a major electron trap as described in the next section.

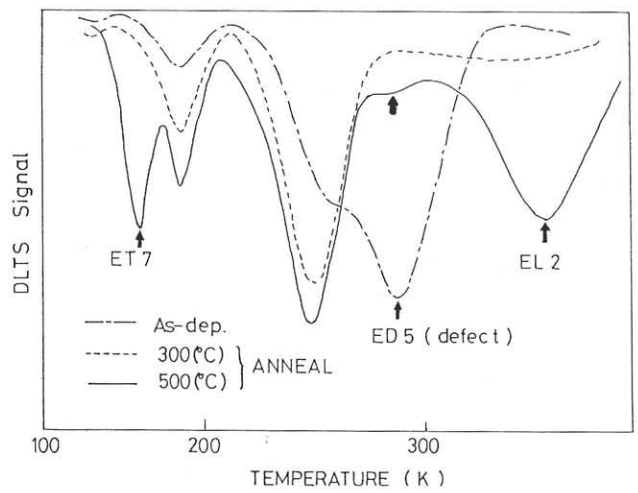

Fig. 2. DLTS spectra for WSi/GaAs Schottky diodes; as-deposited, annealed at 300 °C and 500 °C.

3. Pd/GaAs system

Sample and measurement

Pd was evaporated onto HB GaAs wafers and Schottky diodes were fabricated. The annealing was done in Ar atmosphere at 250 and 300 °C for 30 min. Pd reacts with GaAs to form compound layers[3]. Schottky characteristics and deep levels were measured in the similar method as in Section 2. Au/GaAs Schottky diodes were also fabricated as a control sample.

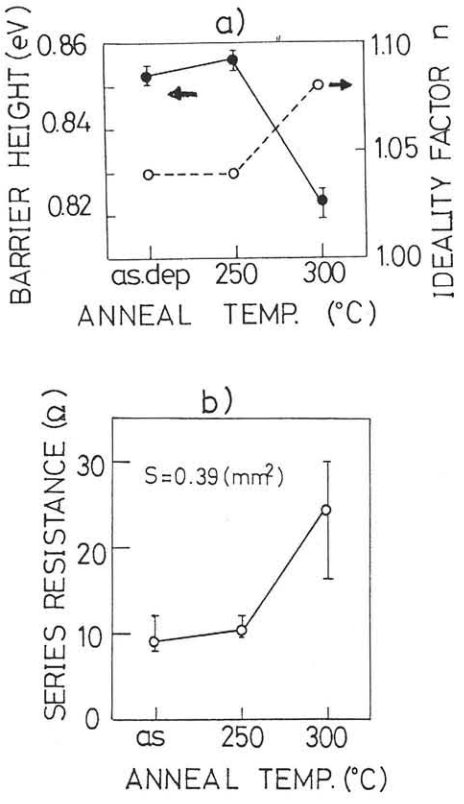

Fig. 3. Change of Schottky characteristics in Pd/GaAs systems.
a) Barrier height (ϕ) and ideality factor (n).
b) Series resistance.

Schottky characteristics

The barrier height, ideality factor and series resistance are shown in Fig. 3. After annealing at 300 °C the characteristics were deteriorated. This is related to change of midgap levels as shown next.

Deep levels

DLTS spectra measured at different bias voltages in three samples; Au/GaAs, as-deposited and 300 °C annealed Pd/GaAs diodes, are shown in Fig. 4. Two major traps were "EL2" and ET7. It is interesting to note that the shape of the spectra for "EL2" is broadened near the interface in all samples and this broadening is largest in the 300 °C annealed Pd/GaAs sample, which shows large ideality factor.

The density profiles of "EL2" are shown in Fig. 5. In an Au/GaAs diode the profile is constant, while in Pd/GaAs diodes, the density decreases toward the inside. Such change of the density profile of "EL2" was reported for Al/GaAs diodes, too.[4)]

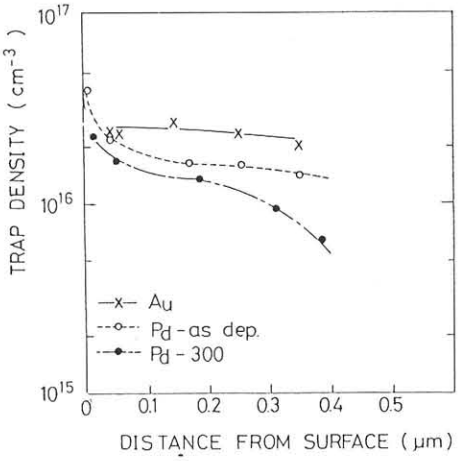

Fig. 5. Density profile of EL2 for Au/GaAs, as-deposited and 300 °C annealed Pd/GaAs diodes.

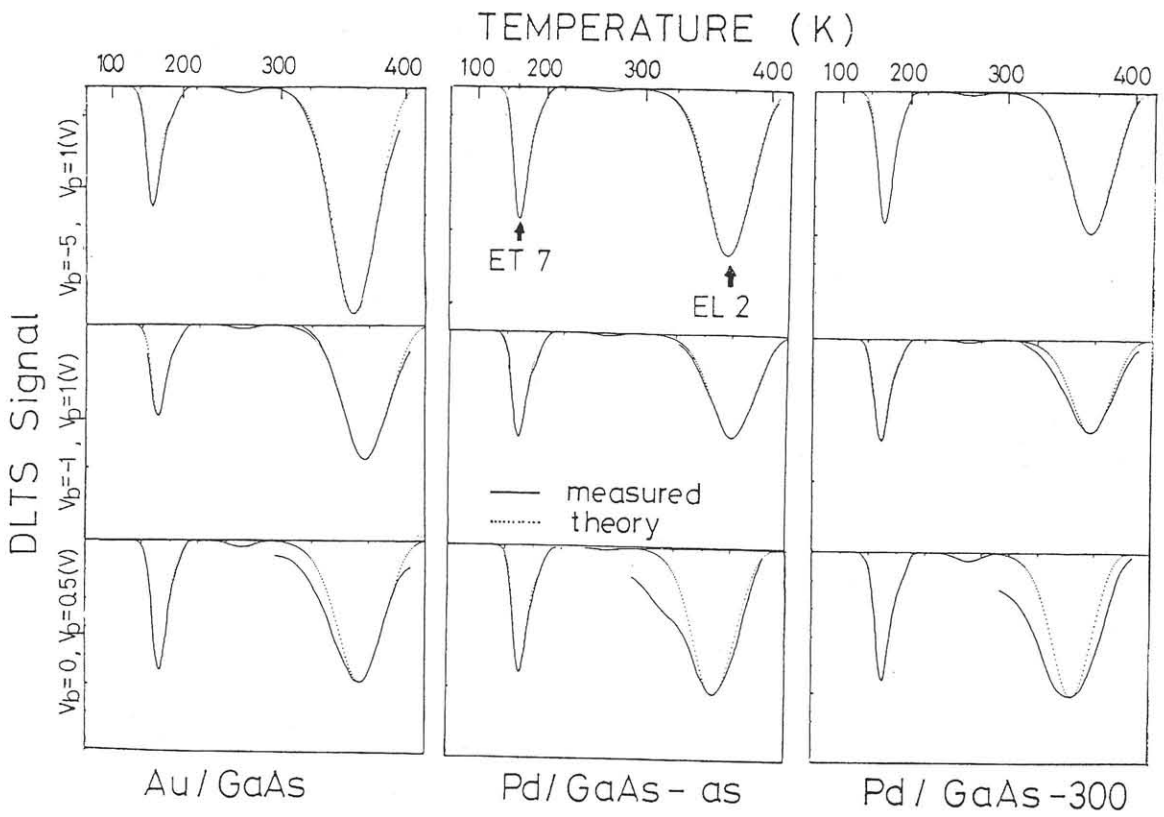

Fig. 4. DLTS spectra measured at different bias voltages; Au/GaAs, as-deposited and 300 °C annealed Pd/GaAs diodes.

4. Discussion

In W-silicide/GaAs systems, sputtering-induced interfacial defect may be responsible partly for degradation of the ideality factor. This defect can be annealed out rather quickly after annealing. At higher temperature annealing another level appeared with low density as seen in Fig. 2. After 700 °C annealing, Schottky characteristics became poor and DLTS spectrum was also distorted very much. This is ascribed to dissociation of As.

Disappearence of "EL2" in the as-deposited samples and re-appearance after annealing at 500 °C and above are very interesting. This is a similar phenomenon as in the oxygen implantation and annealing experiment. [5] Based on our model for "EL2", this is interpreted as follows. Arsenic aggregates, which exist in bulk GaAs and form "EL2 family"[6], depopulate during W-silicide deposition. During annealing, excess arsenic atoms redistribute and create "EL2". Since diffusion of interstitial arsenic atoms can be very fast, the "denuded" zone can extend to rather deep in as-deposited samples.

In Pd/GaAs systems, the change of "EL2" density is noticeable as compared with the Au/GaAs system. This also explained by our hypothetical model as follows. Reaction of Pd with GaAs may extract excess arsenic atoms near the interface and reduce the concentration of "EL2". It is likely that excess arsenic atoms diffuse like Cr which often piles up at the surface during annealing. This may interpret the increasing density of "EL2" near the surface.

The broadening of "EL2" spectrum near the interface is also very interesting. The reaction of Pd with GaAs forms an interfacial layer which can disturb the atomic structure of "EL2". This broadened mid-gap levels are related with the degradation of the ideality factor. It is also interesting to note that even in an Au/GaAs system, the spectrum became broadened near the interface. Such broadening was not observed for ET7 in all the cases.

5 Summary

W-silicide/GaAs and Pd/GaAs systems were investigated in terms of Schottky characteristics and deep level change with annealing. Sputtering induced level was identified and found to have correlation with the ideality factor. The redistribution of "EL2" due to W-silicide and Pd deposition and the annealing, was detected and interpreted by our hypothetical model for the origin of "EL2 family". The broadening of DLTS spectrum of "EL2" was found near the interface.

References

1) N. Yokoyama, T. Ohnishi, K. Odani, H. Onodera and M. Abe, IEEE Trans ED, ED-29 (1982) 1541.

2) N. Toyoda, M. Mochizuki, T. Mizoguchi, R. Nii and A. Hojo, Inst. Phys. Conf. Ser. No.63 (1982) 521.

3) J. O. Ololafe, P. S. Ho, H. J. Hovel, J. E. Lewis and J. M. Woodall, J. Appl. Phys. 50 (1979) 955.

4) A. Yahata and M. Nakajima, Japan. J. appl. Phys., 23 (1984) L313.

5) M. Taniguchi and T. Ikoma, Inst. Phys. Conf. Ser. No.65 (1983) 65.

6) M. Taniguchi, Y. Mochizuki and T. Ikoma, Paper presented at Third Conference on Semi-Insulating III-V Materials, Kah-Nee-Ta, Oregon (1984).