Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 615-618

5.6 ps DCL Gates Fabricated by High-J_C NbN-Oxide-PbIn Josephson Junctions

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High-J_c NbN Josephson junctions were fabricated and their junction properties investigated. The NbN junctions with a J_c value of 2 x 10^8 A/m^2 and junction area of 1.5 μm-square had an I_{min}/I_c ratio of 0.1 and energy gap reduction rate of 4 %. The DCL gate chain was constructed using these high-J_c NbN junctions. The obtained switching delay for the DCL gates was 5.6 ps/gate.

§1. Introduction

Josephson junctions with base electrodes of Nb or Nb compounds show promise for use as digital devices, owing to their high reliability and durability. Their junction capacitance which is higher than that for lead-alloy junctions, however, causes slow switching speed in logic gates. A high-J_c Josephson junction is an effective way to compensate for the high dielectric constant of the Nb oxide. The high-J_c and small area junction will also facilitate response to future demands for greater circuit integration and a shorter switching delay.

However, it will be necessary to clarify the following points when applying the high-J_c Josephson junctions to a logic circuit with the aim of realizing higher switching speed; (1) The method for fabricating high-J_c Josephson junctions and forming fine-patterns. (2) The I-V characteristics for the high-J_c junctions. (3) The J_c range where the logic gate with high-J_c junctions will have adequate switching margins. (4) A high speed sampling method with picosecond resolution. (5) Experimental verification of high switching speed by the high-J_c junction.

This paper reports on the fabrication of high-J_c NbN Josephson junctions 1.5 μm in square as well as on their junction characteristics, especially the minimum-resetting-current and energy gap. The optimum J_c range for high speed logic operations in a latching circuit was pursued based on the characteristic data. A logic circuit chain was constructed using these junctions for purposes of experimentally proving the high speed switching operation.

§2. Experimental Method

The Josephson junctions were fabricated of a Nb-NbN double-layered base electrode 200 nm thick,[1] a Nb oxide tunnel barrier, a SiO masking film and a Pb-5wt.%In counterelectrode 500 nm thick. In order to obtain a small junction window of accurate size and square shape, double SiO masking films with a narrow groove were alternately fabricated so that the grooves of each layer crossed perpendicularly. The junction size was 1.5 μm in square.[2]

A chain circuit was composed of NbN Josephson junctions, Mo resistors and a Nb groundplane for magnetic shielding. The Mo film thickness was 0.1 μm and sheet resistance was 1.0 ohm.

The NbN junction was fabricated as a result of NbN surface cleaning and oxidation steps with a conventional RF discharge in a pure Ar or Ar/O_2 mixture atmosphere. The patterns of the Nb, NbN and Mo films were formed by an ion-etching technique. The SiO and Pb-alloy films were patterned using a lift-off process. The NbN junctions having different J_c values were formed by changing the O_2 content of the gas mixture in the RF oxidation process.

§3. Junction Characteristics

The key parameters for application of Josephson junctions to logic circuits are leakage current, gap voltage, V_g, and minimum-resetting-current, I_{min}. The NbN junctions have a low leakage current owing to their high gap voltage, and a simple oxide barrier structure compared with Nb junctions.

The J_c dependence of the resistance ratio, R_j/R_{nn} (R_j being the quasi-particle tunneling resistance below the gap voltage measured at 2 mV, and R_{nn} being the normal tunneling resistance measured at 6 mV) is shown in Fig. 1. An R_j/R_{nn} value of 17 was obtained below the J_c value of 5 x 10^7 A/m^2. The calculated R_j/R_{nn} value at 4.2 K was 40. The difference between the measured and calculated values may be due to the oxide barrier structure not being uniform.

The structure below the gap voltage in the I-V curve was observed in addition to that at the voltage $(\Delta_{NbN} - \Delta_{PbIn})/e$. The voltages for these structures corresponded to Δ_{NbN}/e and Δ_{PbIn}/e. The current increase at these voltages was stressed for high-J_c junctions. These structures of the high-J_c junctions decreased the R_j/R_{nn} value.

The J_c dependence of the gap voltage V_g is shown in Fig. 2. The gap voltage was 3.9 mV at a J_c range of lower than 5 x 10^7 A/m^2, whereas the gap voltage decreased to 3.2 mV at a J_c value of 1.7 x 10^9 A/m^2. The V_g value shown in Fig. 2 is for a 1.5 μm-square junction. The V_g value for a 2.5 μm-square junction decreased to 2.9 mV at the same J_c value. The energy gaps for both NbN and PbIn electrodes can be derived from the values of V_g and $(\Delta_{NbN} - \Delta_{PbIn})/e$. The energy gap of the NbN film was 5.3 meV, and that of the PbIn film was 2.5 meV, respectively. The energy gap values of both electrode films revealed the same dependence on critical current density.

The energy gap reduction of Josephson junctions is not desirable for logic circuits. This energy gap reduction is accompanied by a critical current reduction. The energy gap reduction for the high-J_c junction originates from nonequilibrium quasi-particles in the voltage state. The critical current recovers to its original value after a time interval equivalent to

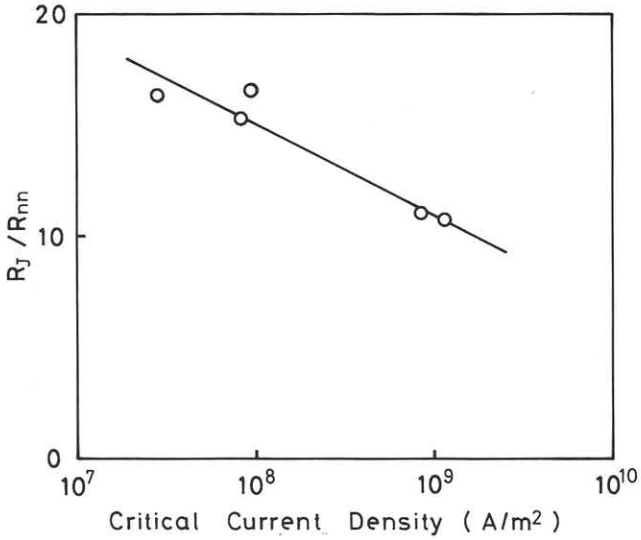

Fig. 1 The R_j/R_{nn} vs. critical current density.

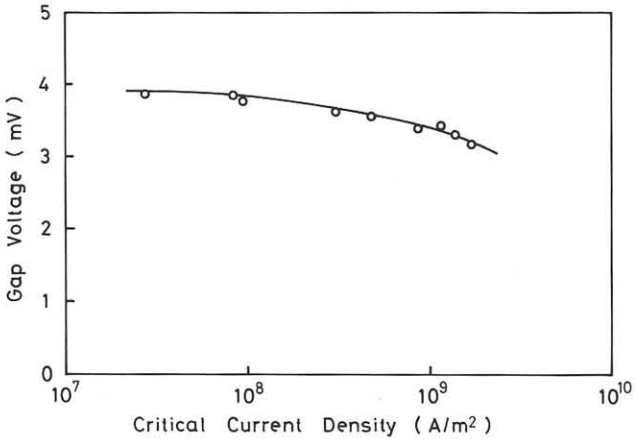

Fig. 2 Energy gap vs. critical current density.

the effective quasi-particle recombination lifetime at the moment the junction resets to a zero voltage state. This lifetime was estimated to be 2.3 ns for a Pb junction.[3] The critical current fluctuates in the logic circuit where the cycle time of the circuit is not adequately longer than the quasi-particle recombination lifetime. Therefore, it is necessary to employ a junction having an adequately small degree of energy gap reduction.

The ratio of the minimum resetting current to the critical current, I_{min}/I_c, depended on the critical current density as shown in Fig. 3. Numerically simulated I_{min}/I_c curves are also shown in the figure. In the simulation, the junction I-V curve was modeled by a piecewise-linear resistor in which R_j, R_{nn} and V_g values were taken into account. The junction specific capacitance, C_j, was chosen as a

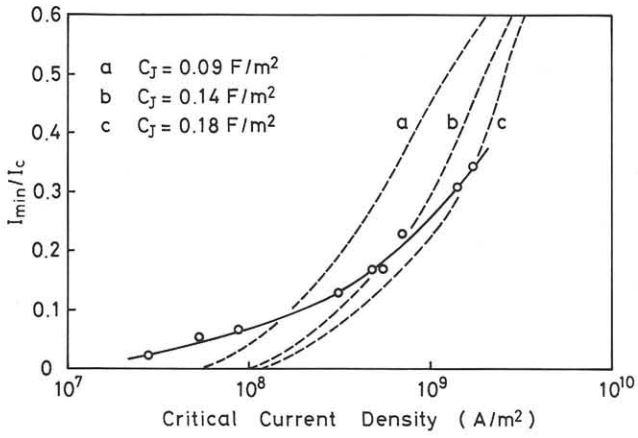

Fig. 3 The I_{min}/I_c vs. critical current density. The open circles indicate measured values. The dotted curves indicate calculated values.

parameter. Each curve corresponds to the specific capacitance of; (a) 0.09 F/m^2, (b) 0.14 F/m^2 and (c) 0.18 F/m^2. These three curves are coincident with the measured I_{min}/I_c value at a J_c value of (a) 2 x 10^8 A/m^2, (b) 5 x 10^8 A/m^2 and (c) 2 x 10^9 A/m^2. Results indicate that the C_j value doubled with a ten-fold increase of the J_c value. The C_j value derived from the resonance step voltage in the I-V curve of a two-junction interferometer also doubled over the same J_c range. This C_j dependence on the J_c does not fit the C_j equation experimentally obtained by Magerlein[4] for the J_c range from 10^7 to 10^8 A/m^2, where the C_j increase was only 16 %.

In the high J_c range, the I_{min}/I_c value was depressed compared with the Pb-alloy junction case due to the high gap voltage, in addition to the high specific capacitance. In the low-J_c range, the I_{min}/I_c value was also depressed due to the high R_j/R_{nn} value.

§4. Gate Delay Time

It is necessary to derive the appropriate J_c range for the latching logic circuit according to the above mentioned junction characteristics. The most critical parameter was the minimum resetting current. In particular, the I_{min}/I_c value has to be sufficiently low in a direct-coupled-logic (DCL) circuit, otherwise the gate may be in a self-resetting mode at the moment the signal current is transferred to a load resistor. The I_{min}/I_c value also determines the signal current transfer rate from one logic gate to its neighbour. To obtain a current transfer level higher than 90 %, the maximum allowable J_c value for the NbN junction is 2 x 10^8 A/m^2. At a J_c value of 2 x 10^8 A/m^2, the R_j/R_{nn} value is 14, and the energy gap reduction rate is 4 %, according to Figs, 1 and 2. Therefore, a NbN junction with the J_c value of 2 x 10^8 A/m^2 is most desirable from the viewpoint of both switching speed and current transfer rate.

The fast-switching capability of a NbN junction with this J_c value was experimentally investigated using a DCL circuit. The DCL circuit was chosen because gate logic delay in that case would consist of turn-on delay, switching delay and propagation delay, but not consist of crossing delay as in the magnetically coupled logic case.[5] A DCL gate does not have a factor of limiting its size, so the gate propagation delay can be made sufficiently small. Therefore, the small time constant of the Josephson junction can be directly reflected to the DCL gate.

The fabricated DCL gate was of the same type as that proposed by Gheewala.[6] This gate consisted of three 1.5 μm-square Josephson junctions, and two resistors, R_1 and R_2. The gate size was 40x40 μm^2. The DCL chain circuit shown in Fig. 4 was constructed for the purpose of measuring gate delay time. The chain circuit had a pulser, an eleven-DCL-gate path, a single DCL gate path, and a sampling gate. The pulser was composed of two DCL gates and had the role of steepening the input signal waveform. The DCL gates were coupled with each other by a load resistor, R_L. The resistance ratio for R_1, R_2 and and R_L was 1:0.43:3. The sampling gate was made up of a two-junction interferometer.

With this circuit construction, the input signal pulse could be divided into two signals. One passed through the eleven DCL gates to the

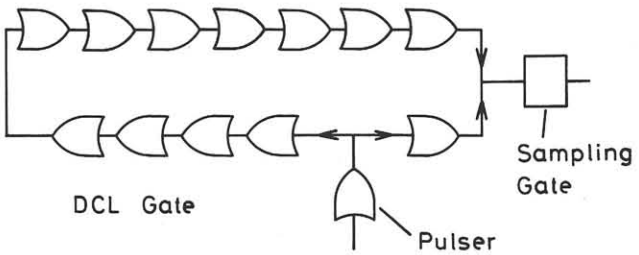

Fig. 4 Diagram of the DCL chain circuit.

sampler, and the other passed through the one standard DCL gate to the sampler. Therefore, two current steps can be detected at the sampling gate. The time interval between these current steps corresponds to the signal delay time for the 10 DCL gates. The output waveform was detected by a typical Josephson sampling method. Details of the measuring method have been explained elsewhere.[7)]

An example of the detected waveform is shown in Fig. 5. The first current step corresponds to the signal through the standard DCL gate, and the second to the signal through the eleven DCL gates. The time interval between the current steps is 56 ps. Therefore, gate delay time is 5.6 ps/gate. The bias current was seperately fed into the

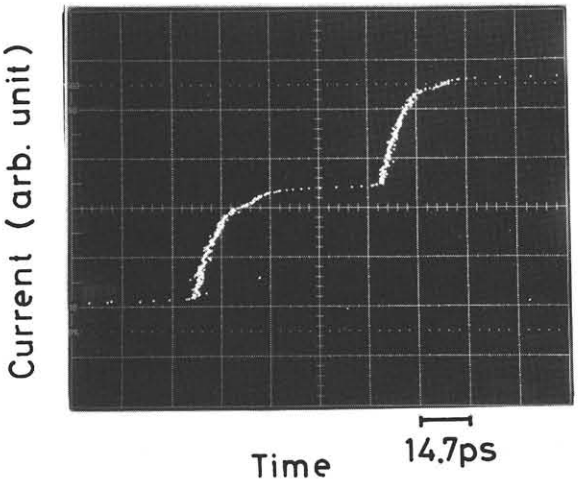

Fig. 5 Output waveform of the DCL chain detected at the sampler.

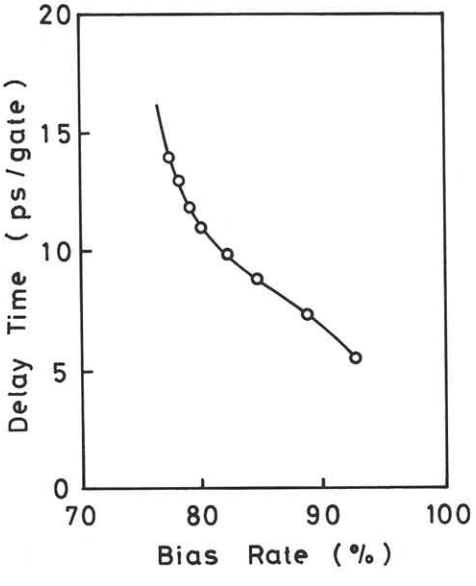

Fig. 6 Gate delay time vs. bias current rate.

standard gate and eleven-DCL-gate-chain. The bias current level for the standard gate was kept equal to the level for the gate having the minimum I_c value among the eleven DCL gates.

Delay time is shown vs. gate bias rate in Fig. 6. The bias current region where the signal current propagated through the eleven DCL gates was from 77 to 92.5 % of the average I_c value. The lower limit of the bias current region was limited not by the static threshold characteristics but by the I_{min} value of the junction. According to the numerical simulation, the delay time was 4.2 ps/gate at the bias rate of 90 %. This experimental result may, however, reveal the high speed switching capability of the high-J_c junction itself.

In conclusion, the high-J_c range where a logic gate has a wide bias margin has been experimentally determined to be at up to 2×10^8 A/m^2 for a NbN Josephson junction. A DCL gate chain was constructed using a NbN junction with a J_c value of 2×10^8 A/m^2, and junction size of 1.5 μm-square. A gate delay of 5.6 ps/gate has been obtained for the circuit.

Acknowledgement

The authors are indebted to Dr. H. Hayakawa and Dr. A. Shoji for passing on the NbN film fabrication technology. The authors would also like to thank Dr. M. Kudo for his encouragement through the work.

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