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A 1k bit Josephson RAM Integrated with Variable Threshold Cells

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A model chip for 1k-bit level Josephson random access memory (RAM) utilzing new type of variable threshold memory cells is designed, fabricated and investigated experimentally. The circuitry was integrated by a 5-μm lead-alloy technology on 5x5 mm chip. The memory cell operations have been performed in the 1k-bit cell array using an external word current input. To evaluate the access time, a delay time of the 1k-bit cell array has been measured and a delay of 1.2 ns was obtained.

1. Introduction

It is important to investigate memory devices for realizing Josephson digital systems. Considerable efforts have been done for integrating Josephson memory chips using various types of cells.[1-3] We have already proposed a single flux-quantum memory cell which utilizes a new type of variable threshold, and demonstrated the operation of the cell.[4] The memory cell has many attractive features for integrating the cells. The cell can be accessed with only two lines, X and Y, in the word organization with a large operating window, which allows us to integrate the cells closely and to simplify the peripheral circuits. Another important feature is that the NDRO operation can easily be achieved by adding simple loop drive circuits in the cell arrangement. In this paper, we report a design of the memory cell and experimental results of a model chip for 1k-bit RAM integrated by a 5-μm lead-alloy technology.

2. Memory Cell and Operation Principle

Figure 1 shows a schematic configuration of the memory cell. The memory cell has an equivalent asymmetric dc SQUID structure in which J_1 is a 3-junction SQUID gate and J_2 is a single junction. L is the inductance of the memory loop. The word current I_X is applied to the cell as the control current for J_1 gate. Hence the maximum gate current of J_1 is changed as a function of I_X. The critical current of J_2 is chosen to be equal to the maximum current of J_1 without the control current I_X. The bit current I_Y corresponds to the gate current of the equivalent asymmetric dc SQUID. L is designed as LI_0 becomes about Φ_0, where $\Phi_0=2.07\times10^{-15}$ Wb is one flux quantum. The information is stored in the memory loop as a flux quantum for a "1" and as the absence of flux quantum for a "0".

A typical threshold curve of the cell is shown in Fig.2. The vertical axis corresponds to the maximum current of I_Y and the horizontal axis corresponds to I_X. The dotted line represents the vortex transition region. The "0" state is stable in the region between the lines "0", while the "1" state is stable in the region between the lines "1". One of the advantages of this memory cell is that an NDRO operation can easily be performed by adding a simple circuit in a cell arrangement. Figure 3 shows a bit line arrangement for the NDRO operations. I_G is a dc power to bit lines. Y and R are the input pulses to the set gate J_Y and the reset gate J_R, respectively. M_i is a memory cell and I_{Xi} is the word current to the cell M_i. A sense gate J_S is coupled magnetically to the bit line and senses the bit current I_Y. The memory cells are serially connected in a superconductive loop which contains a set gate J_Y and a reset gate J_R. The set gate is used to transfer a dc current I_G to a bit line for generating I_Y, while the reset gate resetting I_Y.

In this configuration, memory operations are explained as follows. For writing a "0", the word current I_X is applied, which decreases I_{01}. If a "0" is stored, the J_1 gate does not switch. But if a "1" is stored, J_1 switches and the stored flux quantum is lost because LI_{01} becomes so small that the cell cannot trap a flux quantum any longer. For writing a "1", first I_X is applied and followed by the bit current I_Y. This makes J_1 switch and then I_Y flows into the J_2 branch. Consequently a flux-quantum is trapped in the cell after switching I_X, afterward I_Y off. Every transition from "1" to "0" or from "0" to "1" in the writing processes is a vortex transition; therefore, no stationally voltage is generated across the cell except voltage spikes.

For reading, first I_Y is applied and followed by I_X. If a "0" is stored, the reading process causes to cross the threshold of the voltage transition, making the cell switch into the voltage state. In order to assure the NDRO operation in this sequence, I_X should be turned off after switching I_Y off. In the cell arrangement shown in Fig.3, these operations can be automatically achieved, because I_Y is transferred back to the set gate due to the voltage transition of the cell itself before I_X is turned off.

If a "1" is stored, there exists a clockwise circulating current in the memory loop, cancelling a current flowing through J_1, which is too small to switch the J_1 gate and the cell remains in the zero voltage state. For the NDRO operation, I_X should be turned off before removing I_Y in this sequence. These operations can be made by switching the reset gate to reset I_Y after I_X is turned off.

Since all cells to which I_X is applied implement the operation of writing of a "0", this type of memories is suitable for the word organization rather than the bit organization, which ensures the simplicity of the cell and the peripheral circuits.

3. 1k-bit Level Integration

Shown in Fig.4 is a block diagram of the RAM chip. The circuitry consists of a 64x16bit memory cell plane, a 4bit-to-16output decoder, sixty-four drivers and sixteen sense circuits. The memory plane consists of sixteen superconductive bit lines. In each bit line, sixty-four memory cells, a set gate and a reset gate are serially connected as shown in Fig.3.

The decoder circuits are organized with direct-coupled Josephson logic gates, the 4JL gates.[5] The decoder is a two-stage AND decoder connecting 24 unit cells. A unit cell is constructed with two OR gates, an AND gate and an

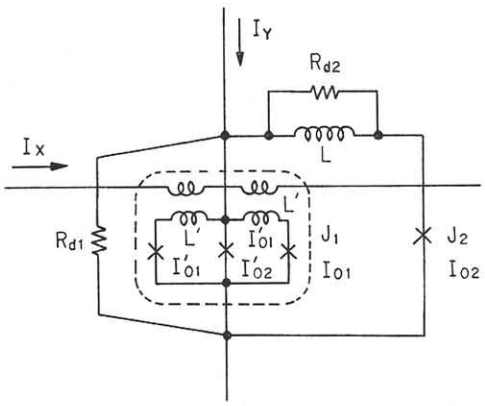

Fig.1 Schematic configuration of the variable threshold memory cell.

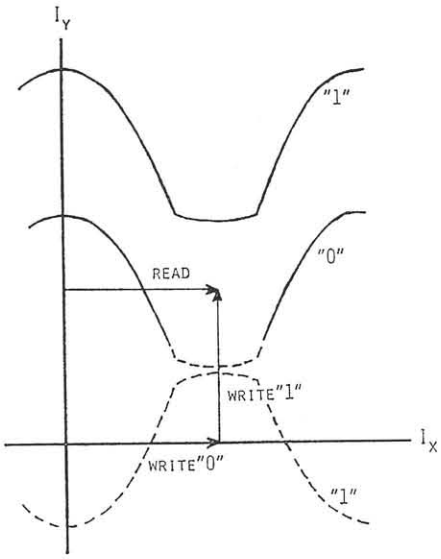

Fig.2 Threshold characteristic of the cell.

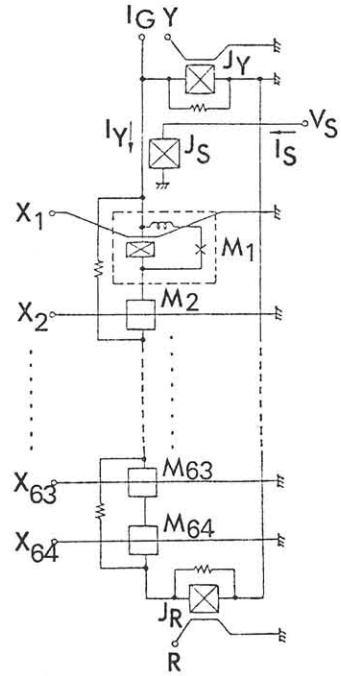

Fig.3 Schematic diagram of one bit line.

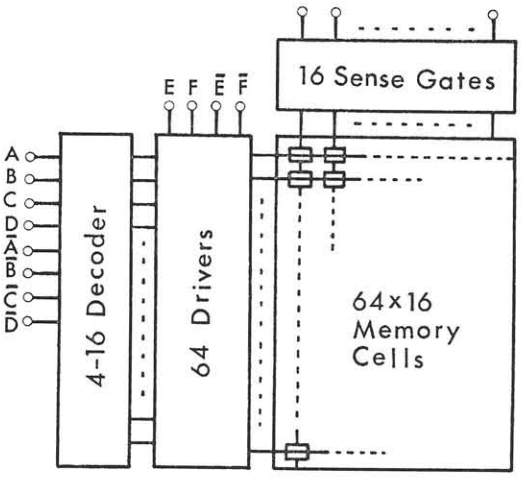

Fig.4 Block diagram of the 1k-bit RAM.

amplifier gate to have a fanout of 4. In the first stage, two AND outputs are generated from two pairs of inputs. In the second stage, an AND output is generated from the two AND outputs out of the first stage.

The signals A, B, C, D and their complements are four upper address bits to the decoder. The output from the decoder and two lower address bits E, F are the inputs to the drivers. A driver has a function of 2-input AND and drives the word line of the memory plane. The driver is a center-fed 3-junction SQUID gate with a large operating window as large as ±26%. The set and reset gates are designed on base of the center-fed 3-junction SQUID gate. Their maximum gate current is chosen to be larger than the operational bit current I_Y of 0.4 mA by a factor of 1.4. The sense gate is also a center-fed 3-junction SQUID gate with a relatively large mutual inductance, so that it can

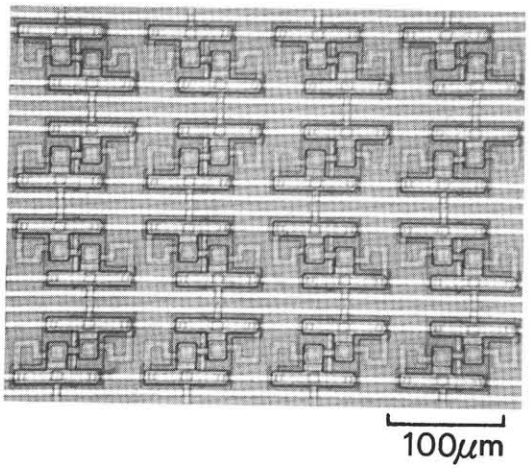

Fig.5 Photomicrograph of the integrated variable threshold memory cells.

detect the change of I_Y more than 0.3 mA with the operating margin ±50%.

For the proper flip-flop operation of the bit line, damping resistors in the set and reset gates should be appropriately selected. The damping resistors are determined by computer simulations to be 6Ω for a bit line loop with the inductance of 300 pH.

Devices were fabricated using a lead-alloy integration process with a 5-μm minimum linewidth. A photomicrograph of the integrated memory cells is shown in Fig.5. The size of a cell is 105x40 μm.

Figure 6 shows a photomicrograph of the fabricated 1k RAM chip. The chip size is 5x5 mm.

The operation of the 4JL decoder has been separately performed. The operating characteristics of the decoder will be published elsewhere. Figure 7 is one of the traces obtained by the memory operation for one cell in the cell array. After each write operation three NDRO signals are obtained. The proper read/write operations were performed. But in this experiment, an external word current input was used as I_X. The reason is that on this fabricated chip, the required current level for I_X was so high that the output of the 4JL decoder could not drive the I_X driver.

To evaluate the access time of the 1k RAM, a

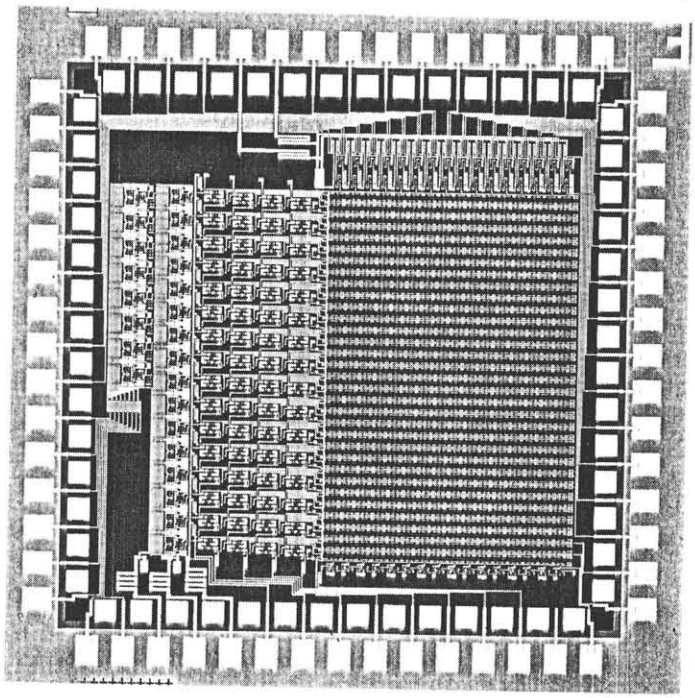

Fig.6 Photomicrograph of the 1k-bit RAM.

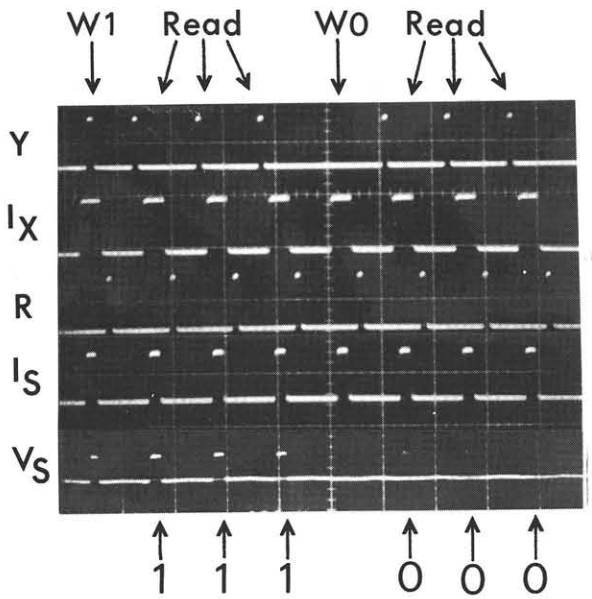

Fig.7 Experimental result of memory operations of a cell in 1k-bit array. (horizontal:20μs/div.)

delay time from the I_X driver to the sense gate through the critical path, as shown in Fig.8, is measured. In Fig.8 different from Fig.3, the dc power I_G is fed to the bit line at the point between the memory cells and the sense gate. Therefore the sense signals obtained in this configuration is inverted from the signals shown in Fig.7, and by applying I_S after the set pulse Y, the readout signal out of a "0" state cell makes a voltage across the sense gate J_S immediately. A delay time of 1.2 ns was obtained

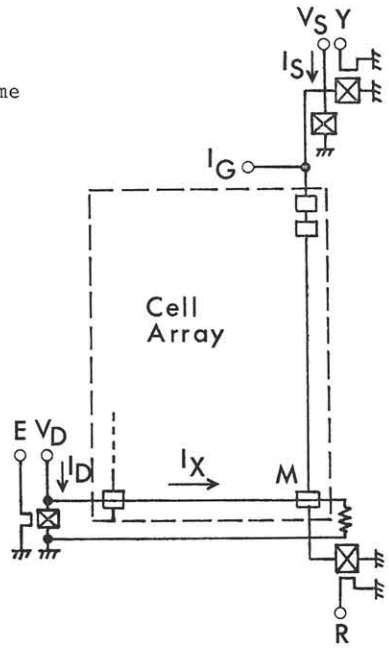

Fig.8 Delay time of 1k-bit cell array for the critical path (between the driver monitor output V_D and the sense output V_S) has been measured.

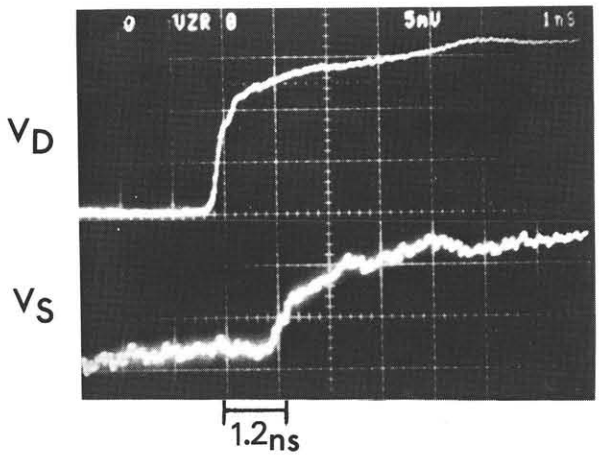

Fig.9 An experimental result of the delay measurement for cell array. The faster and the slower traces correspond to a driver monitor output and a sense output, respectively.

as shown in Fig.9. The delay time of the 4JL decoder is evaluated to be about 300 ps from the measurement of the delay time of the 4JL unit cells. From these data, the access time of the 1k RAM is estimated to be about 1.5 ns.

5. Concluding Remarks

A model chip for 1k-bit level Josephson RAM integrated with new type of variable threshold memory cells has been made with a 5-μm lead-alloy technology. The memory operation has been performed for a memory cell in the cell array using an external word current input.

To evaluate the access time of the 1k-bit RAM, the delay time for the critical path between the driver monitor output and the sense gate output has been measured. The delay time of 1.2 ns was obtained. Adding the delay time of the 4JL decoder to this delay, the access time of the 1k-bit RAM is expected to be 1.5 ns.

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