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Current Injection Josephson Latch Circuit

T. Yamada, J. Sone, and S. Ema

Microelectronics Research Labs., NEC Corporation
4-1-1 Miyazaki, Miyamae-ku, Kawasaki 213, Japan

A novel ac powered current injection Josephson latch circuit is presented. Data are stored in it as a circulating current in a superconducting loop which contains two Josephson junctions. Data are read out by an interferometer gate directly to the loop. The proper operation was verified in the experimental latch fabricated using a 5 μm Pb alloy Josephson technology. The device size is 300 x 300 μm^2, which is a tenth of that of a magnetic coupled Josephson latch with the same feature size.

1. Introduction

Josephson devices are attractive ultrahigh-performance computer elements. Their high performance is based on the high switching speed, low power dissipation and the impedence matched superconducting transmission line inherent to the Josephson technology. These features have been demonstrated by various types of Josephson logic circuits(for example, see 1)-3)).

In order to construct the logic circuit, latch circuits are necessary to store data during the time interval when an ac power supply changes its polarity. Various kinds of the latch circuits have been reported[4)-6)]. Most of them use magnetically coupled interferometer circuits. Because of the magnetically coupled transformers used, these circuits may occupy relatively large areas on the chip. In previous papers reported[2),3)], we have discribed a family of current injection logic circuits, which bear significant advantages over the magnetically coupled logic circuits in both size and speed. We propose in this paper a novel current injection Josephson latch circuit in order to construct a complete current injection logic circuit.

In this circuit, data are stored as a circulating current in a loop which consists of two serially connected junctions and an inductance. A two-junction interferometer gate is directly coupled to the master circuit and reads out the stored data. The dual rail signals are generated by Josephson junctions and RCJL(Resistor Coupled Josephson Logic) gates using the data read out by the sense gate. This latch circuits is experimentally fabricated using a Pb alloy Josephson technology with a 5 μm minimum feature size[5)].

2. Latch Circuit Operation

The basic current injection latch circuit is shown in Fig. 1. It has a master-slave configuration. The master circuit is designed to write the data at the flat portion of the power supply and to hold the data during the time interval when the ac power supply changes its polarity. The slave circuit is designed to read the data stored in the master circuit during the power supply ramp and to hold the data at its output until the end of the machine cycle. The latch circuit is designed based on a 5 μm Pb alloy Josephson technology. A Josephson current density of 800A/cm^2 is chosen for the design. Typeical circuit parameters are shown in the figure.

2-a. Master Circuit

The master circuit consists of two RCJL OR gates G_1 and G_2, a RCJL AND gate D_2, and a superconducting loop. The loop is composed of two serially connected junctions J_2's and inductances L_1 and L_2. L_2 is directly coupled to an interferometer sense gate Q_1.

The write operation of the master circuit is described below. First, a latch enable signal (LE) is injected into the loop and the gate G_2. G_2 switches and an output current delivered to D_1. When a data signal (DATA) is activated, G_1 switches and an output

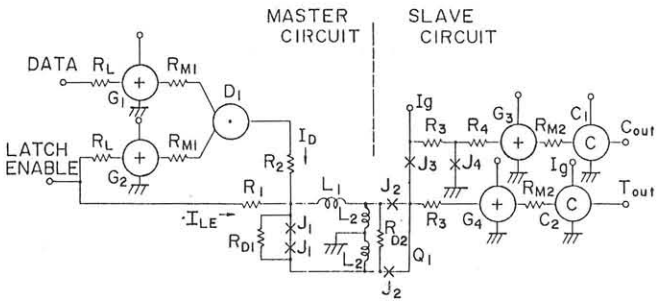


Fig.1. Equivalent circuit of the latch circuit
I_1=0.3mA, I_2=0.15mA, I_3=I_4=0.22mA, L_1=13.4pH, L_2=2.4pH, R_{D1}=1ohm, R_{D2}=2ohm.

current is injected to the loop, causing magnetic flux to enter the loop. Thus the data is written as a circulating current in the loop.

The relationship betweeen the phase difference θ of the junction J_1 and the current I injected to the loop is shown in Fig. 2. Current injection into the loop from the slave circuit side is prohibited in the write operation because either a junction J_3 in the slave circuit or the gate Q_1 switches into the resistive state, as explained later in the slave circuit operation. In the figure, a solid line shows the characteristic with the junction J_3 in the resistive state, and a broken line shows the characteristic with the gate Q1 in the resistive state.

In this design, two junctions are inserted into the storage loop in order to accomplish the magnetic flux generation of $\sim 2\phi_0$ in the loop when the data signal is activated. That is,

$$I_1(L_1+2L_2)\sim 2\phi_0 \ ,$$

where I_1 is the Josephson critical current of the junction J_1 and ϕ_0 is a magnetic flux quantum. Hereafter, this operation is referred to as $2\phi_0$-mode operation. The $2\phi_0$-mode operation is adopted in this design to make the operating margin wider.

The reason why the $2\phi_0$-mode makes the operating margin wider is as follows. If a single junction is used in the loop, the ϕ_0-mode operation is realized with a relationship of

$$I_1(L_1+2L_2)\sim \phi_0 \ .$$

In order to maximize the operating margins of the sense gate, the inductance L_2 has to satisfy the relation,

$$I_{cir}\cdot 2L_2\sim \phi_0/2 \ .$$

where I_{cir} is the amplitude of a circulating current generated in the loop, and is nearly equal to I_1. Thus, L_1 becomes comparable to L_2 in the ϕ_0-mode operation, and difference in I-θ characteristic in Fig. 2 between the solid line and the breken line becomes noticeable. It results in the decrease of the operating current margin of the DATA and the LE signal.

In the absence of the current injected into the loop, B, A, C in Fig. 2 are stable operating points. As explained in the following, the operating point stays at either B or A when the power supply had the negative polarity in the previous machine cycle. In order to reset the storage loop, the latch enable signal is applied in the next cycle, then the operating point moves from B or A to D. When the DATA signal is applied subsequently, the operating point moves from D to F through E, and magnetic flux is caused to enter the loop. On the other hand, the operating point stays at D if the DATA signal is not applied. At the end of the machine cycle, all signals are removed. Then, the operating point moves to C in case of DATA "1", while it moves to A in case of DATA "0". Similar operations are repeated in the following cycle with negative polarity. Thus, DATA "1" is represented by the states at point B or C, depending upon the power supply polarity. DATA "0" is represented by the state at point A. From the value of θ at B and C, the amplitude of the circulating current I_{cir} can be estimated as

$$I_{cir} = I_1 \sin\theta = 0.22 \text{ mA}.$$

Fig.3 shows that the DATA signal and the LE signal have as much as ±40% of the operating current margin.

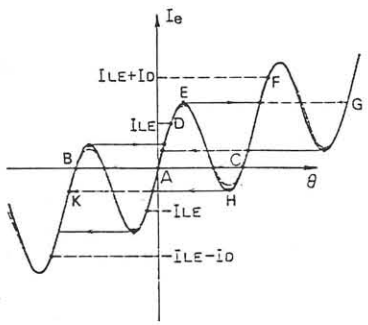


Fig.2. I-θ characteristic curve

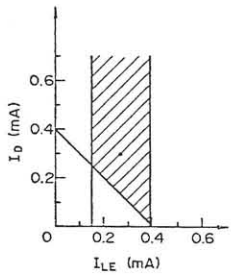


Fig.3. Current margins

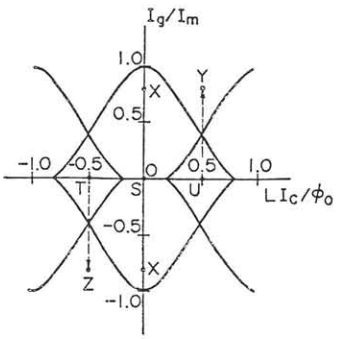
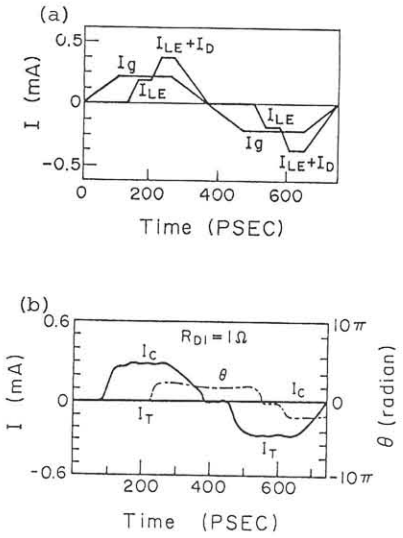


Fig.4. Threshold characteristic of the Q1 gate



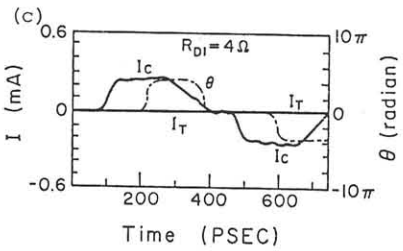


Fig.5. Results of the computer simulations

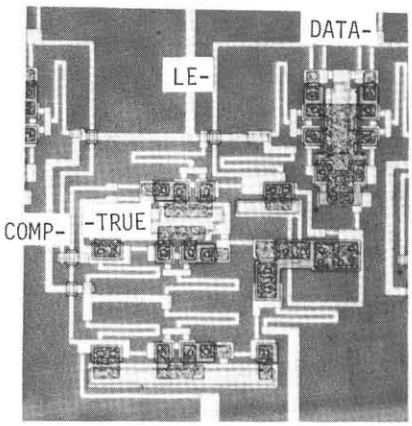


Fig.6. Photograph of the experimental latch circuit

2-b. Slave Circuit

The slave circuit consists of a junction J_3 with a critical current of I_3, a junction J_4 with a critical current of I_4, the sense gate Q_1, RCJL OR gates G_3, G_4 and current amplifiers C_1, C_2. The critical currents I_3 and I_4 are chosen to satisfy the relationship of

$$I_g^0/2<I_3=I_4<I_g^0\ ,\ I_m(I_{cir})<I_3=I_4<I_m(0)\quad ,$$

where I_g^0 is the gate current in the flat portion of the power supply, $I_m(0)$ and $I_m(I_{cir})$ are gate threshold currents of the gate Q_1 in the presence and absence of the circulating current in the loop, respectively.

When DATA "1" is stored in the form of a circulating current, Q_1 switches before J_3 during the power supply ramp and an output current is injected into G_4 and J_4. Then G_4 and C_2 switch in this sequence, providing "1" at the true output. On the other hand, J_3 and J_4 remain in the superconducting state, and the output on the complement branch is "0". Since Q_1 and G_4 operate in a latching mode, these ouptut states remain unchanged even if the circulating current changes its value during the same cycle. When DATA "0" is stored in the loop, J_4, G_3, and C_1 switch in this sequence, providing "1" at the complement output. In the same time, the supply current to Q_1 is diverted to a resistor R_3. This prevents Q_1 from switching even if DATA "1" is later entered in the latch during the same cycle.

The threshold curve of Q_1 is shown in Fig. 4. S, T, U show the operating points of Q_1 in the absence of the gate current. Here S corresponds to the operating point when no circulating current is present in the loop, while T and U corresponds to the operating points when the nominal circulating current is present. These points moves to X, Y, and Z in the figure, when the gate current is applied. Thus, we can see that Q_1 switches only when the circulating current is present.

3. Computer Simulation

The amount of the magnetic flux generated in the loop deeply depends on the damping resistance R_D. In order to realize the $2\phi_0$-mode operation, proper value of the damping resistance has to be chosen by the simulation. Fig. 5 shows the results of the two cycle computer simulation. The power supply rise time of 100 psec was chosen for the simulation. The input DATA sequence is "1","1". The LE signal is activated every cycle before the arrival of the input DATA. The simulation begins with zero stored in the latch circuit. Fig. 5(b) shows the proper operation of the latch circuit with R_D = 1 ohm. The proper operation was maintained with the power supply rise time as small as 50 psec. The punchthrough occured with the power supply rise time smaller than 50 psec. As shown in Fig. 5.(c) as a typical erroneous case, the

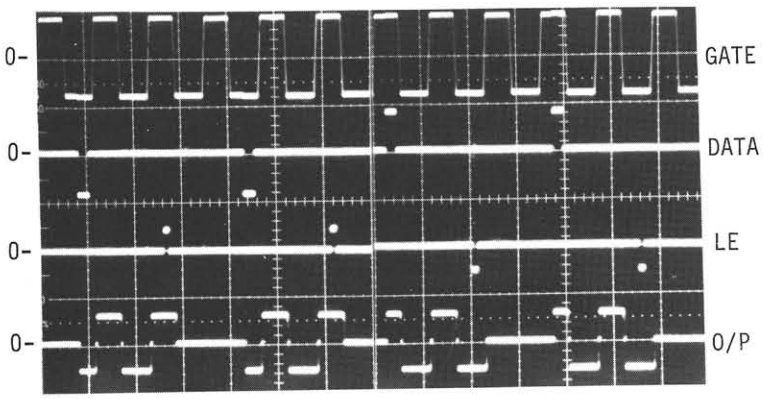


Fig.7. Experimental operation of the master circuit

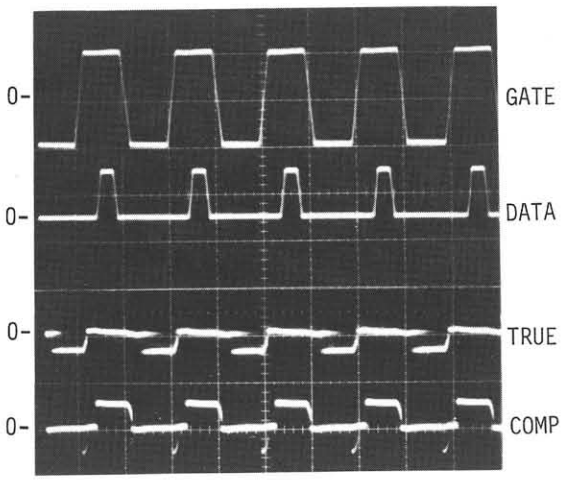


Fig.8. Experimental operation of the latch circuit

circuit with damping resistance R_D larger than 4 ohm operates improperly. It is because the shifts of the operating point from E to G and from H to K occur. The damping resistance of 1 ohm is chosen in this design.

4. Experiments

The current injection latch circuit was fabricated using a 5 μm Pb alloy technology. A photograph of the latch circuit is shown in Fig. 6. This device includes a LE signal generator[7] in addition to the circuit in Fig. 1, and is capable of producing the latch enable signal automatically. The latch circuit occupies an area of 300 x 300 μm^2, which is a third of that occupied by a magnetic coupled Josephson latch circuit with a 2.5 μm minimum feature size. The latch circuit has nine power supply lines and the total power dissipation at the droping resistances of 42 ohm in the latch is about 34 μw.

The experimental operation of the master circuit is shown in Fig. 7. The DATA signal and the latch enable signal are directly injected into the storage loop. The output voltage of the gate Q_1 is measured. The master circuit is powered by an alternating trapezoidal waveform. The data signal produces a circulating current in a storage loop. From the next cycle on, output signals are generated. Then, the LE signal resets the storage loop and no output signals are generated from the next cycle on.

Fig. 8. illustrates the proper operation of the latch circuit with the LE signal generator. The DATA "1" were applied in the positive cycle and the DATA "0" were applied in the negative cycle. We can see that data are read out in the following cycle.

5. Conclusion

A new Josephson latch circuit has been proposed which operates by the ac power supply. The experimental latch circuit was fabricated and the proper operation was verified. The device size was 300 x 300 μm^2, which can be estimated to be nearly a tenth of the interferometer circuit with the same feature size. The complete current injection logic circuit system can be constructed by combination of the present latch circuit and current injection logic gates such as the RCJL family.

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