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AC Powered Master Latch Circuit with Complementary Outputs

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Abstract

Conventional latch circuits allow only small tolerances because of the complex operation of slave circuits. Wider operating margin is obtained if a master latch stores both the output of a logic circuit and its complement signal. We propose an AC powered master latch circuit with complementary outputs. The proposed master latch circuit was fabricated and a wide operating margin, ±40%, was obtained.

1. Introduction

Josephson logic circuits operate in a latching mode. These latching logic circuits must be reset to zero voltage state at the end of the logic cycle by lowering the supply current to zero. This is achieved by using a trapezoidal AC power supply[1] which also acts as the master clock of the whole system. The outputs of the logic network are stored in latch circuits before the power supply begins to fall.

A latch circuit is composed of a master latch (ML) and a Self Gating AND (SGA) circuit (See Fig. 1). ML stores the data during the AC power supply transition time, and SGA detects the stored data at the beginning of the next cycle. Conventional latch circuits have a narrow operating margin because detection of the data by SGA is a rather complex operation.

In this paper, we report the design and experimental evaluation of a novel master latch circuit which provides a wide operating margin. In Section 2 we discuss problems with the conventional master latch circuit and propose a master latch circuit with complementary outputs. In Section 3 more precise design is discussed and Section 4 shows experimental results.

2. Operation mode of master latch circuit with complementary outputs

Figure 1(a) shows the operation mode of a conventional AC powered latch circuit.[2] ML stores only DATA and SGA generates T^* and C^*. In Fig. 2(a), typical equivalent circuit of SGA and movements of operating points are shown. The operation is as follows,

(1) When T=1, operating point of Q1 is at A at the beginning of cycle time. As the bias increases, Q1 switches first and SGA operation is executed.

(2) When T=0, the operating point is at B. As the bias increases a Josephson junction J switches first instead of Q1, and the outputs $T^*=0$, $C^*=1$ are obtained.

From the above explanation it is clear that two conditions must be satisfied for correct operation, that is,

$$Im_0 > I_J \qquad I_J > Im_1$$

These conditions are rather stringent when there are variations in circuit parameters. Therefore, SGA operation allows only a narrow operating margin compared with combinatorial logic circuits. This discussion can be applied qualitatively to other SGA circuits of this type.

Figure 1(b) shows another type of latch operation where ML stores both DATA and $\overline{DATA}$.[3] Figure 2(b) shows the equivalent circuit of SGA which receives the two outputs. Let the operating points of Q1 and Q2 be at A and B, respectively when T=1 and C=0. As the power supply rises, Q2 switches first and the outputs $T^*=1$, $C^*=0$ are

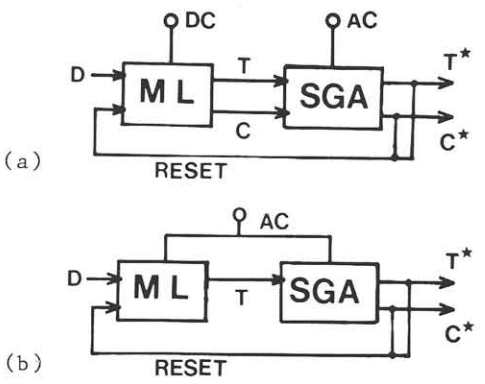

Fig. 1 Mode of latch operation
(a) DC power type
(b) AC power type

obtained. In this case, only one condition, i.e., $Im_0 > Im_1$ is necessary for correct operation. Thus, a latch circuit of this type has a wider operating margin than the conventional latches. However, the conventional master latch circuit which stores both DATA and $\overline{DATA}$ is operated by DC supply power. This is not desirable because combinatorial logic circuits are operated by AC supply only.

So, we have investigated a master latch circuit which can be driven by an AC supply alone.

3. Design of the proposed master latch

Figure 3 is the equivalent circuit of the proposed master latch circuit. Operation is as follows.

(1) After the sense gates SG1 and SG2 detect the stored data, delay gate DG and gate AMP for current amplification are switched. Then, gate WG1 has only control input and WG2 has both control input and bias current which is supplied through gate TG. So, independent of data of the preceding cycle, circulating current flowing through WG1 is reset to "0" level.
(2) If the data is "0", circulating current is stored in WG2 at the end of the cycle. So, "1" and "0" are written in WG2 and WG1, respectively.
(3) If the data is "1", then TG is switched and current I_T is transferred to resistor R2 and circulating current in WG2 becomes "0". Data current I_D becomes bias current of WG1.

So, the circulating current is stored in WG1 at the end of the cycle. "1" and "0" are written in WG1 and WG2, respectively.
DG is used to delay the reset current I_R which must be applied after SGA reads the stored data. Write gates WG1 and WG2 should have low enough so-called floor current to obtain a large difference between "1" and "0". But the SQUID with the lower floor current has less sensitivity. This problem had been avoided by winding control lines two times over the SQUID. Such a design, however, increases the size too much in this case where two write gates are used. So, a single turn control line for input after current amplification by the AMP gate was adopted.

Figure 4 shows the computer simulated operating margin of the proposed master latch circuit. (In computer simulations bias current rise time was assumed to be 100 ps. This corresponds to 1 ns cycle time with 80 percent active ratio.)

The operating margin is determined by the following conditions,

(1) Current flowing through gate TG must be lower than the maximum critical current of TG.
(2) The operating point defined as (I_G, I_D) must be beyond the threshold of TB.
(3) The number of stored magnetic flux quanta in the Write Gate corresponding to "1" level must be greater than the ones corresponding to "0" level.

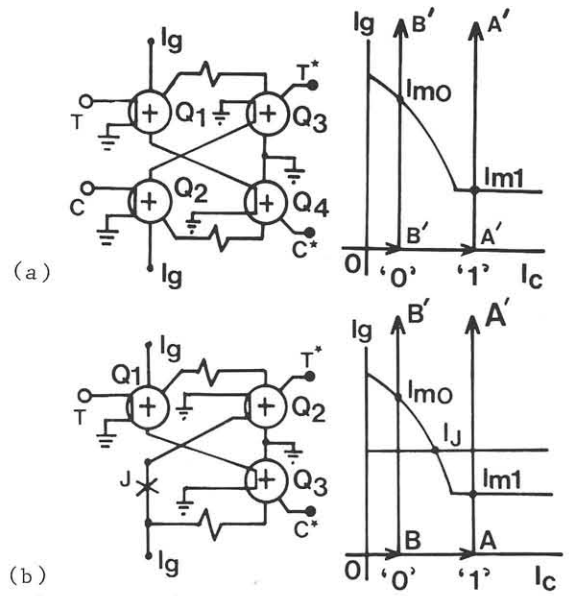

Fig. 2 Operation of SGA at rise of AC power supply
(a) AC type
(b) DC type.

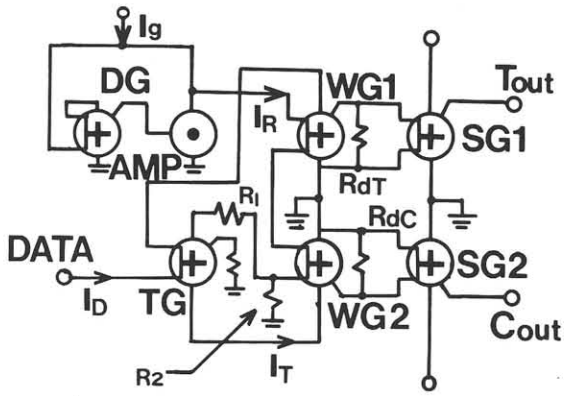

Fig. 3 Equivalent circuit of the proposed latch
⊕ and ⊙ denote 3JSQUID and RCJL, respectively.

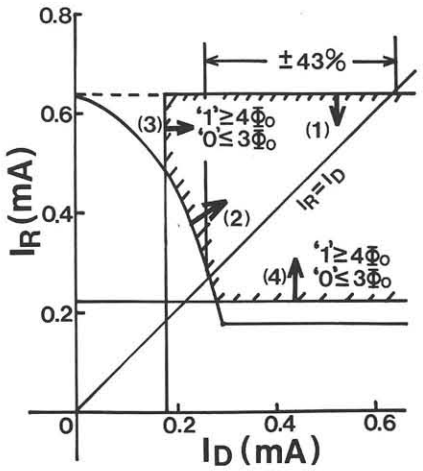

Fig. 4 Operating region of the proposed latch.

Condition (1) determines the maximum of I_G and (2) and (3) determine the minimum of I_G and I_D. These conditions are shown in Fig. 4 with their numbers. The design values of the circuit parameters are summarized in Table 1. The operating margin is estimated to be ±43%. It is noteworthy that this value is the same as margins of the CIL Gate Family.

4. Experiments

The proposed latch circuit was fabricated using Pb-alloy technology. The minimum feature size was 4 μm. Figure 5 is a photograph of the fabricated master latch circuit. The area occupied was 0.075 mm^2. Circulating currents stored in write gates are sensed by SG1 and SG2. The magnitudes of the circulating currents were measured by the shifts of threshold characteristics to horizontal directions. Figure 6 shows an example of correct operation waveforms. If D is "1" in the preceding cycle, Tout=1 is generated at the rise of sense gate bias current I_S, and if the data is "0", Cout is generated before Tout when I_S rises. Thus, correct operation is obtained.

Figure 7 shows the region of I_G and I_D exhibiting such correct operation. Assuming I_D to be 80 percent of I_G (This is a typical transfer ratio of signal to bias current), operating margin of ±40% is obtained. This is almost the same as the design value.

These experiments were performed with the sense gate bias I_S set at 0.5 mA. From the measured threshold characteristics it is known that a circulating current more than 0.15 mA is necessary to switch the sense gates. In Fig. 8 bias current dependence of circulating currents is shown. From these results $I_D \geq 0.4$ mA and $I_G \geq 0.15$ mA are necessary to obtain circulating currents more than 0.15 mA. These minimum values of I_D and I_G agree well with the I_{G}th, I_{D}th shown in Fig. 7.

5. Conclusion

A novel master latch circuit with complementary outputs was proposed. It has a wider operating margin than previously proposed circuits. The circuit is composed of two rfSQUIDs operating in parallel, therefore it is operated by the same AC power as the combinatorial logic circuits and is latch-up free.

The proposed master latch circuit was fabricated and the expected wide margin, ±40% was obtained. This measured margin includes the sense operation. Thus, almost the same value of operating margin can be obtained for a whole latch circuit by designing SGA circuit adequately.

Rd	1.5Ω	R1	3Ω
R0	1.5Ω	R2	0.5Ω

	TG	DG, WG
I_0	0.126mA	0.1mA
L_b	2.6pH	1.3pH

Table 1 Designed values of circuit parameters.

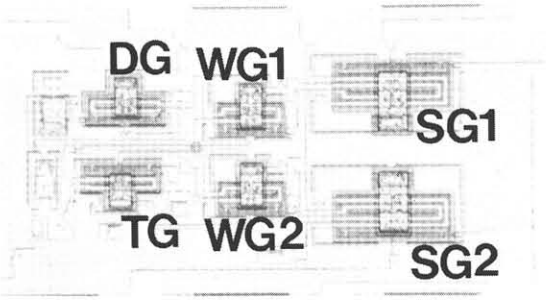

Fig. 5 Photograph of the fabricated latch circuit.

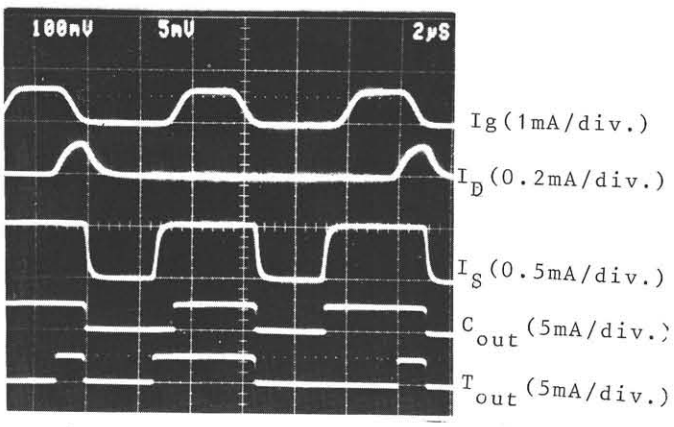

Fig. 6 Pulsed operation of the latch.

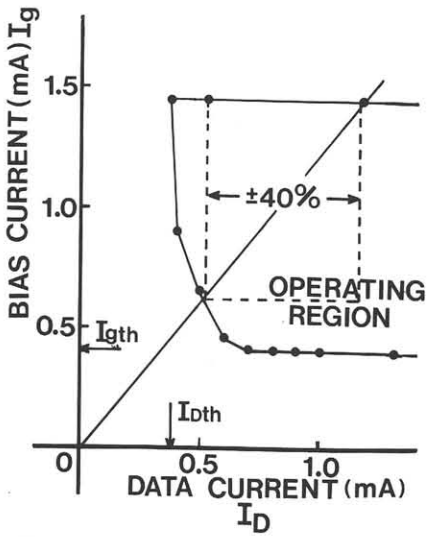

Fig. 7 Measured operating region of the fabricated latch circuit.

Acknowledgement

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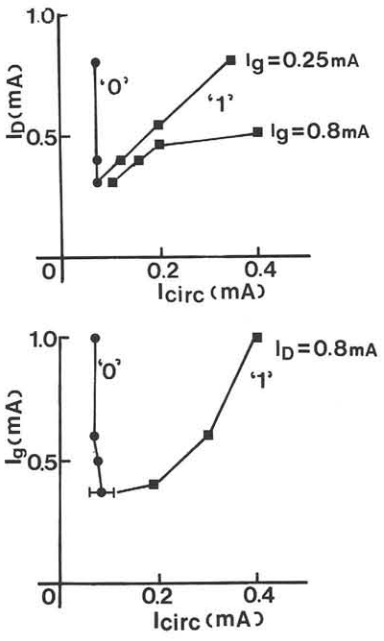

Fig. 8 Measured circulating currents stored in
(a) WG1
(b) WG2..