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RF CO_2 Oxidation and Double-Layer Resist Technique Realizing Josephson Junctions Very Small I_j-Spread

Jun'ichi Nakano, Yoshiaki Mimura, Koichi Nagata, Yuji Hasumi and Takao Waho

Atsugi Electrical Communication Laboratory, N.T.T.

1839 Ono, Atsugi, Kanagawa, 243-01, Japan

New techniques for fabricating Pb-alloy Josephson junctions with a very small I_j spread are proposed: rf oxidation in CO_2 plasma for high controllability and stability of barrier oxide, and double layer resist technique for accurate definition of the junction window by a lift-off process. These techniques make it possible to obtain a small I_j spread of σ = 6.8% for 2x2 μm^2 junction area and a very fast switching delay of 4.2ps/gate in current injection type logic gates.

1. Introduction

Logic circuits using high switching-speed Josephson tunnel junctions are attractive for digital application. With a current injection type logic RCL[1)], a switching speed of 6ps/gate was achieved using Pb-alloy junctions with an area of 3x3μm^2 and a current density of 2kA/cm^2. To realize larger scale integration of the gates using a smaller junction area, the junction current I_j must have a very small deviation from the target value.

In this paper, we present new fabrication techniques: rf oxidation in CO_2 plasma for high controllability and stability of barrier oxide, and a double-layer resist technique for accurate definition of the junction window by a lift-off process.

To evaluate these techniques, they were used to form Pb-alloy junctions. The scattering of I_j in a series of 1000 junctions as well as the switching delay of RCL gates having a 2x2μm^2 junction area was measured.

2 Rf Oxidation in CO_2 Plasma

2-1 Effect of CO_2 in O_2 discharge

Barrier oxide of Pb-alloy Josephson junctions has been formed by rf O_2 plasma oxidation. In the process of investigating oxidation conditions, it was found that CO_2 gas in the O_2 plasma affected I_j and the leakage current of the junctions. Current density of the junctions has a large dependence on the CO_2 concentration which is inevitably released from organic photoresist and the chamber wall. Generally, to prevent this impurity gas effect, the oxygen flow rate during oxidation is kept very high. In the case of the Pb-alloy junction, however, a decrease in the CO_2 concentration results in an increase in the leakage current in the subgap voltage region of the junctions. Therefore, the reproducibility of the current density and quality of the junctions are balanced only by a strict control of the CO_2 concentration.

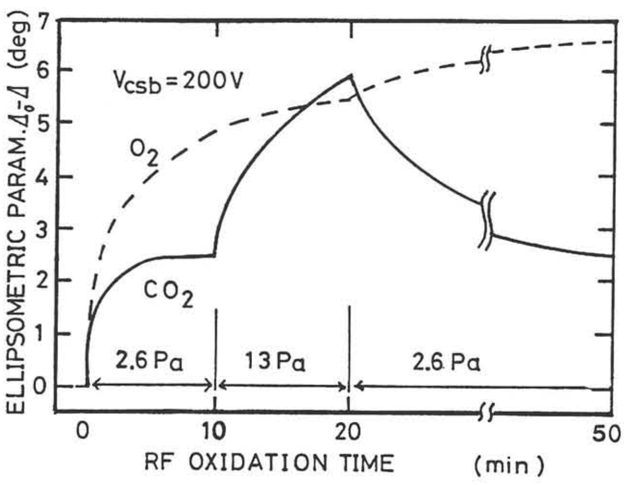


Fig.1 Change in oxide thickness due to rf oxidation in CO_2 and O_2 plasma.

Plasma analysis by optical emission and quadrapole mass spectroscopy showed that CO_2^+ ions play an important role comparable to O_2^+ in the growth of the oxide. On the basis of this analysis, we carried out the oxidation of a Pb-alloy in rf CO_2 plasma and obtained junctions with excellent quality reproducibly.

2.2 Characterization of CO_2 oxidation

(1) Swift saturation of oxide thickness: Figure 1 shows change in the ellipsometric parameter, which has a close relation to oxide thickness, during rf oxidation in CO_2 and O_2 plasma. Steady state oxide thickness is attained in CO_2 plasma more quickly than in O_2 plasma and oxide thickness changes reversibly with pressure, which warrants a high controllability of current density. This swift saturation of oxide thickness was obtained in a relatively low pressure region of less than 4 Pa. Therefore, it is thought that this saturation originates from an increase in the sputtering rate during rf oxidation.

(2) Low leakage current: The high flow rate of CO_2 during oxidation suppresses impurity effects of other gases such as H_2O without increasing the leakage current. Therefore, rf CO_2 oxidation makes it possible to reproduce high quality junctions. The typical R_{SG}/R_{NN} ratio with a current density of 10kA/cm^2 was 11 and the run-to-run reproducibility of the current density was within 7%.

(3) Suppression of I_j changes resulting from heat treatment: Figure 2 shows the relative change in I_j as a result of heat treatment at 70°C. The current increase in the junction oxidized in CO_2 plasma almost stops after annealing for 10 hours at 70°C, while the change in the junctions oxidized in O_2 plasma continues to increase even after 100 hours of annealing. A current increase of less than 5% between 10 to 100 hours might be applicable for large scale gates because annealing for 100 hours at 70°C corresponds roughly to storage at room temperature for 10 years.

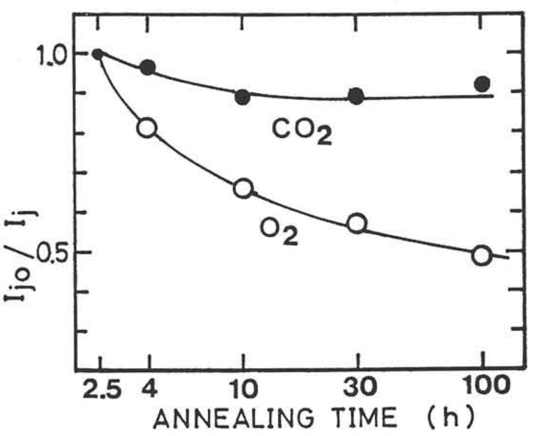


Fig.2 Change in I_j due to annealing at 70°C.

3 Lithography for Small Junction Window

A reduction projection printing technique using a 1/10x wafer stepper as well as a high performance lift-off technique(SHULOT, based on swelling of resist stencil and high frequency ultrasonic treatments) were employed to fabricate the junction window. When the single-layer lift-off stencil, which employs a conventional chlorobenzene soak process[2] was used, the dimensions of the junction window were significantly affected by uncontrollable process conditions: light-scattering from the Pb-alloy base electrode, defocus and irregular distribution of light intensity in projection printing, irregular

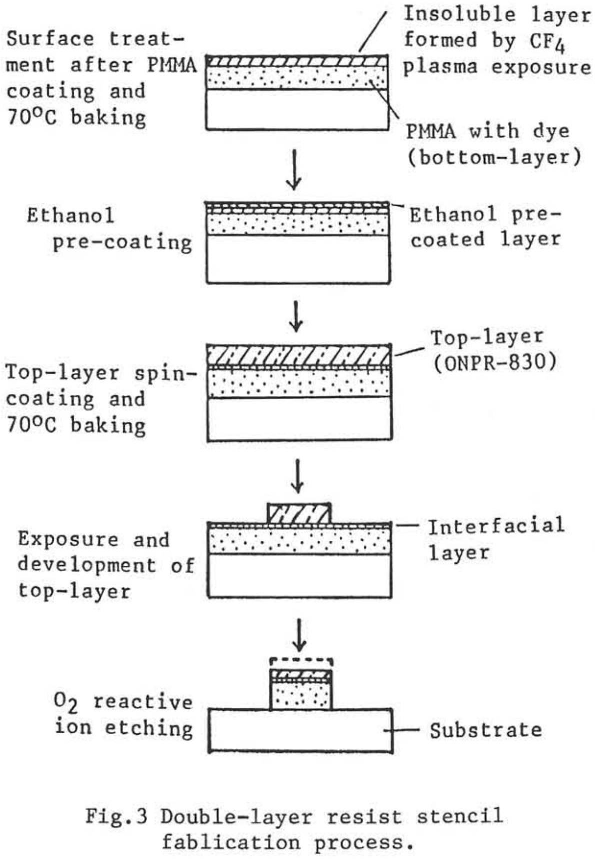
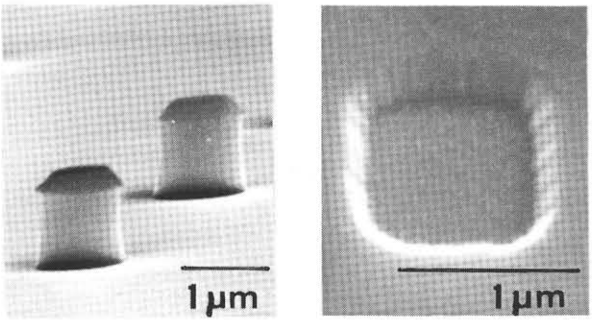


Fig.3 Double-layer resist stencil fablication process.



(A) (B)

Fig.4 SEM photographs of resist stencil(A) and junction window(B) formed by the double-layer resist technique.

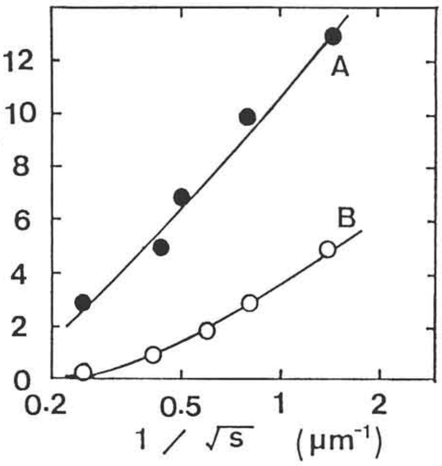


Fig.5 Standard deviation σ of junction window area S vs. junction dimension $1/\sqrt{S}$ formed by conventional(A) and the double-layer(B) techniques.

thickness of modified layer resulting from the chlorobenzene soak. Therefore, it is difficult to fabricate a small junction window with small areal scattering by using the single-layer stencil.

3.1 Double-layer resist stencil

In order to obtain a small junction window with high precision, we developed a double-layer resist stencil system employing a low temperature ($70^{\circ}C$) process for the Pb-alloy. This process is illustrated in Fig.3. The stencil is composed of ONPR-830 for the top layer and PMMA with dye for the bottom layer. The dye in the PMMA bottom layer efficiently absorbs the 436nm wavelength light exposing the top layer and eliminates the influences of light reflected from the base electrode.

The key factor in developing the low temperature process in the double-layer resist stencil system is to control the interface between the top and bottom layers. This is because PMMA baked at $70^{\circ}C$ is easily dissolved by the solvent for the top layer. An indistinct interface having an irregular thickness decreases the accuracy of the top-layer pattern dimension. The key factors in this process are as follows: (1) ONPR-830 resist is employed for the top layer, since cycropentanon, the solvent for this resist, has little effect on PMMA(bottom layer). (2) The surface of the PMMA bottom layer is changed to be insoluble with respect to the top layer solvent as a result of CF_4 plasma exposure. (3) Ethanol is spin-coated on the PMMA layer just before coating the top layer to form a uniform contact between the two layers. (4) The top layer pattern exposed by the wafer stepper is precisely transferred to the PMMA layer by reactive ion etching in O_2. An overhang structure for lift-off is formed by the difference in the etch rate for the two resist layers(etch rate ratio of PMMA/ONPR830 is about 2.5/1.).

3.2 Scattering in junction area

SEM photographs of a stencil and SiO lift-off window fabricated by the double-layer resist stencil technique are shown in Fig.4. A small junction window area is measured with a 20000x or 35000x magnified SEM photograph. Figure 5 shows the relation between the square root of the window area S and the standard deviation σ of the window area. The standard deviation of the 2x2 μm^2 window area, fabricated by the double-layer technique is about 2%, while that obtained by the conventional single-layer technique is about 7%.

4 I_j Scattering in a Series Junction

To evaluate the above techniques, they were used in fabricating a series of 1000 junctions with a chip area of 1x1 mm^2. Small I_j-spread of σ=6.8% with 2x2 μm^2 junctions (Fig.6) was obtained. This spread is smaller than typical spread of 10% for junctions formed by the conventional method. However, there remains a relatively large difference between the I_j-spread and the scattering in the junction area, which is presumably brought about by the inhomogenity of the tunnel barrier. If we can decrease this

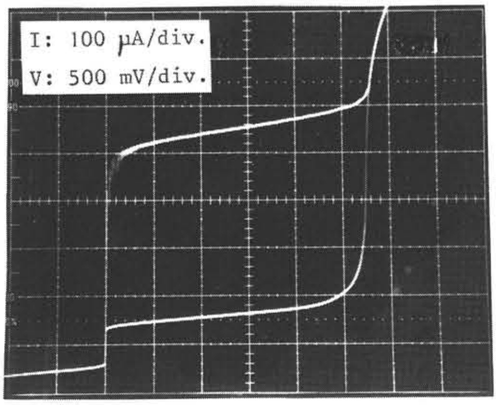


Fig.6 Typical I_j spread for 1000 junctions with $2x2\ \mu m^2$ area and $12kA/cm^2$ current density.

difference, it will be possible to obtain an I_j-spread of less than 3% in $2x2\ \mu m^2$ areal junctions.

5 Switching Delay in RCL Gates.

Using the $2x2\ \mu m^2$ junctions, a chain of 7 RCL gates was fabricated and the switching delay was measured by means of a Josephson sampling technique. Figure 7 shows an illustration of an RCL gate and a block diagram of the circuit. Output signals I_{01} and I_{02} from the first and last gates were detected by the sampling gates.

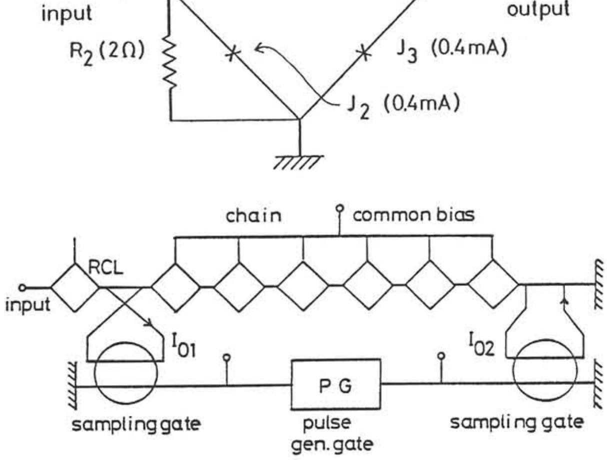


Fig.7 Illustration of an RCL gate and block diagram of a delay measurement circuit.

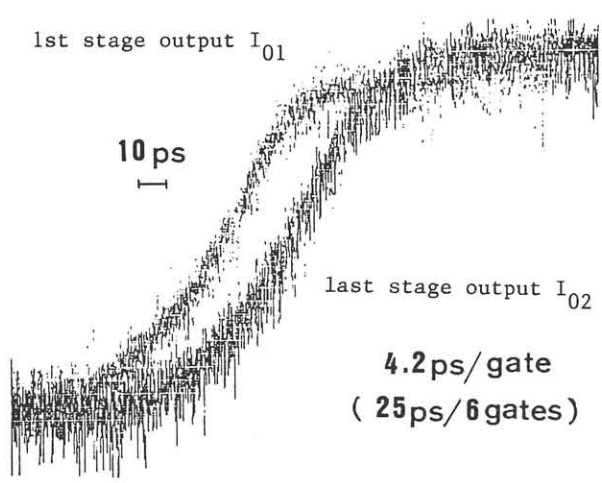


Fig.8 Experimental rise-time waveform in I_b=o.72mA.

Figure 8 shows an experimental rise-time waveform from the gates when about 90% of the common bias current was injected into the gates. A delay time of 4.2ps/gate, which is the fastest among the delays reported to date, was obtained.

6 Conclusion

New fabrication techniques for Pb-alloy Josephson junctions are presented. Rf oxidation in CO_2 plasma resulted in an R_{SG}/R_{NN} ratio of 11 at a 10 kA/cm^2 current density and a I_j increase of less than 5% due to 70^oC-annealing between 10 to 100 hours. A double-layer resist technique makes it possible to use junctions having a very accurate window area: areal scattering of 2% in $2x2\ \mu m^2$ junctions.

Using these techniques, we obtained a I_j-spread of σ= 6.8% in a 1000 junction series. A switching delay of 4.2ps/gate was obtained for this chain of RCL gates.

Acknowledgement

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References

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