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# High-Tolerance Uni-Lateral Single-Flux-Quantum Logic Gate

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A new type of single flux quantum logic gate is proposed which can perform uni-lateral propagation of signals without a need of three-phase clock. An optimum circuit with maximum operating margin was found by varying design parameters to get it larger than 50% with respect to the bias current. Three cascaded gates were modeled and simulated on a computer, and uni-laterality of signal flow was confirmed.

## 1. Introduction

Josephson junction devices provide excellent potential for high-performance computer devices. Single flux quantum logic[1-3] devices in particular are very attractive because of their very high switching speed and extremely low power consumption. Single flux quantum logic circuits, which have been proposed so far need a three-phase clock to ensure the uni-lateral propagation of signals.

In this paper, we propose a new type of single flux quantum logic gate which can perform uni-lateral propagation of signals without a need of three- phase clock. This circuit is designed to use bridge-type Josephson junctions without hysteresis in their current-voltage characteristics, and is promising as a high-speed logic gate because of the small capacitances of the bridge-type junctions.

## 2. Basic gate and operational principles

### 2-1 Basic gate configuration

The basic logic gate consists of two one-junction interferometers coupled by superconducting lines, as shown in Fig.1, where $\lambda_i$ is the characteristic phase of the inductor $L_i$ given by next equation.

$$\lambda_i = 2\pi L_i I_o / \Phi_o$$

The asymmetry of the bias current results in uni-lateral signal flow. Figure 2 (a) and (b) show the calculated threshold characteristics of the gate shown in Fig.1 for the parameters listed in the figure captions, respectively. The method used to calculate the threshold characteristics was to consider the stability condition for the potential energy of the gate.[4] The numbers in the parentheses represent the number of fluxoid quantum in each loop, where a positive sign represents the fluxoid quantum associated with clockwise circulating current and a negative sign represents the fluxoid quantum for the reverse direction. The sum of these numbers must be zero owing to the flux quantization condition in the outer inductance loop.

### 2-2 operational principle

The principle of operation is as follows. Without the input current Ic there is no fluxoid

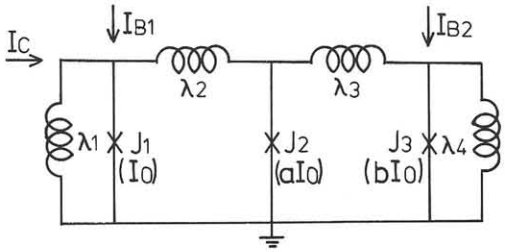


Fig.1 Proposed logic gate; $J_1$, $J_2$ and $J_3$ are Josephson junctions, $I_0$ is the critical current of $J_1$, $I_{B1}$ and $I_{B2}$ are bias current, a and b are constants.

quantum in any loop, or (0,0,0,0) mode; this represents logical state "0". The input current causes $J_1$ to switch, and generates an anti-clockwise circulating current in the leftmost loop and a clockwise circulating current in the adjacent loop. This clockwise circulating current causes $J_2$ and $J_3$ to switch in succession, resulting in a transfer of the fluxoid quantum to the rightmost loop, or (-1,0,0,1) mode; this represents logical state "1".

The coupling between the basic gates can be accomplished by mutual inductance, or its T transform, in the latter case a part of the clockwise circulating current is injected in the next gate to cause the same mode transition. Without the bias current, the gate is in the (0,0,0,0) mode as shown in Fig.2 (a), therefore, resetting the gate to logical "0" state can be accomplished by reducing bias current to zero, similar to the resetting commonly used in Josephson logic gates made from tunnel junctions. In this case, however, Josephson junctions are not in the voltage state, therefore, "punchthrough" which is inherent in Josephson-tunneling logic gates[5] cannot happen.

2-3 Design consideration

Circuit parameters, such as the ratio of the critical current of Josephson junctions and inductances were chosen to make the operating margin with respect to the bias current and the inclination $\Delta I_{B2}/\Delta I_C$ in the threshold characteristics largest. This inclination is related to the isolation between the input and the output, if it is large enough, the change of the phase difference across the output junction causes little effect in the input junction. Uni-lateral propagation of signal can be accomplished without $J_2$-the role of $J_2$ is to make the operating margin with respect to the bias current large, keeping the $\Delta I_{B2}/\Delta I_C$ sufficiently large. If the products of the critical current of $J_2$ with $L_3$ and $L_4$ are chosen properly, a circulating current can be made not to flow in the middle two loops, which means the region in the threshold characteristics corresponding to the modes (-1,1,0,0) and (-1,0,1,0) which are not related to the logical state can be made small, and the operating margin

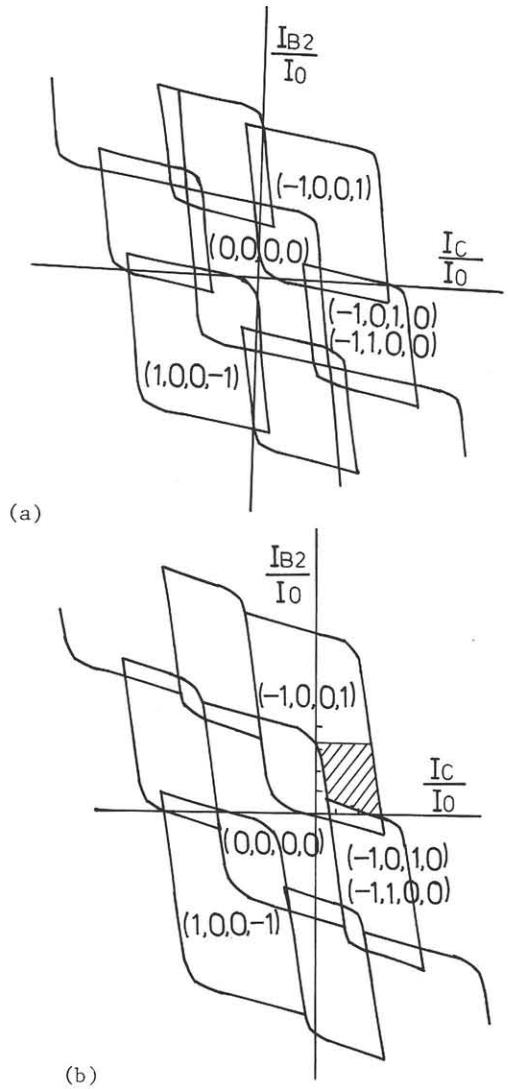


Fig.2 Calculated threshold characteristics for the gate in Fig.1, for two parameters value. The parameters are; (a) a=0.5, b=2, $\lambda_1=\pi$, $\lambda_2=\lambda_3=2\pi/3$, $\lambda_4=\pi/2$, and $I_{B1}=0$. (b) a=1, b=2, $\lambda_1=9\pi/10$, $\lambda_2=\lambda_3=3\pi/10$, $\lambda_4=9\pi/20$, and $I_{B1}=2.0I_0$.

with respect to the bias current becomes larger. Figure 2 (b) shows the calculated threshold characteristics of the optimum gate, indicating that the operating margin is larger than 50% with respect to the bias current $I_{B2}$.

3. Stability consideration of the gate

In the presence of the thermal noise, it is known that thermally activated switching of Josephson junctions may take place.[6] In the mechanical analogy, the behavior of the phase difference across the Josephson junctions can be visualised by a particle moving in a phase-plane.[7,8] In the case of the gate shown in Fig.1, in contrast to the dc SQUID, there is only one potential well in the whole phase-plane corresponding

to one quantum mode, and the case of a particle rolling steadily corresponding to the voltage state does not occur.

Contour maps of potential energy for the gate were calculated in order to study the stability of the gate. The potential energy u is given by the next equation.

$$u = \frac{\Phi_o I_o}{2\pi}\left[1-\cos\phi_1+a(1-\cos\phi_2) + b(1-\cos\phi_3) - (i_c+i_{B1})\phi_1 - i_{B2}\phi_3 + \frac{1}{2\lambda_1}\phi_1^2 + \frac{1}{2\lambda_2}(\phi_1-\phi_2)^2 + \frac{1}{2\lambda_3}(\phi_2-\phi_3)^2 + \frac{1}{2\lambda_4}\phi_3^2\right]$$

where, $\phi_i$ represents the phase difference across the Josephson junction $J_i$.

The hatched region in Fig.2 (b) shows the operating region of the gate shown in Fig.1, where only one stable point exists in the phase-plane, as shown in Fig.3. With the bias current and input current, therefore, the gate is sure to settle down to (-1,0,0,1) mode. Without the input current, however, the operating point is in the overlapping region of (0,0,0,0) and (-1,0,0,1) modes, and in the presence of thermal noise the undesirable mode transition from (0,0,0,0) to (-1,0,0,1) mode may take place. Figure 4 shows the contour map of the potential energy in the overlap region of the two modes for the parameters given in the figure caption. In this figure, there are two stable points at A and B corresponding to the mode (0,0,0,0) and (-1,0,0,1), respectively. The path of easiest escape is from A to B through C, and the potential difference between A and C is about 0.06 eV, which is sufficiently large enough to ensure that the mean time between failure for the system containing $10^6$ gates is longer than one year, in the presence of the thermal noise at 4.2 K. Even though the thermal noise at 4.2 K is considered in the design of the operating bias point for the gate, the operating margin for the gate in Fig.2 (b) is as large as 50% with respect to the bias current $I_{B2}$.

## 4. Computer Simulation

Three cascaded gates shown in Fig.1 were modeled and simulated on computer, where bridge-type Josephson junctions were modeled with a resistively shunted junction model in the limit of heavy damping. The relevant equations are that for fluxoid quantization in each loop and current continuity at each node. The existence of a fluxoid quantum in any one-junction interferometer is represented by the change about $2\pi$ of the phase difference across the Josephson junction contained in that interferometer.

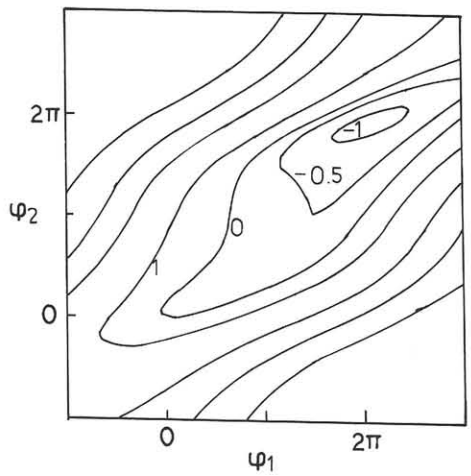


Fig.3 Contour map of potential energy for the gate in Fig.1, with the bias current and the input current. The parameters are the same as in Fig.2 (b), and $I_{B1}=2.0I_0$, $I_{B2}=2.3I_0$ and $I_C=0.7I_0$. The number in the figure shows the value of potential energy for $I_0=50\ \mu A$.

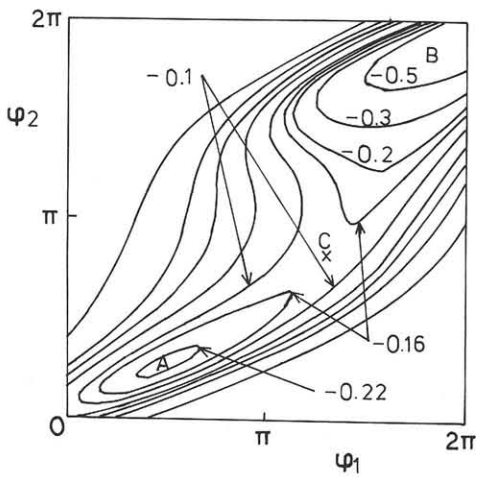


Fig.4 Contour map of potential energy for the gate in Fig.1, with the bias current. A and B are the stable points and C is the saddle point. The parameters are the same as in Fig.3, except for $I_0=0$.

Figure 5 shows the results of computer simulation indicating the forward transfer of a fluxoid quantum, when $I_C$ is applied to the input junction of the first gate. It can be seen that a switching delay about 2 picoseconds per gate is feasible, when $I_C$ overdrives about 20 percents.

Figure 6 shows the results of computer simulation indicating that a pair of flux quanta is generated in the third gate when larger $I_C'$ is applied to the output junction of the third gate, but it does not propagate to the preceeding gates.

Thus, the uni-laterality of signal flow was confirmed from the results of computer simulation.

## 5. Conclusion

We have proposed a new type of single flux quantum logic gate which can perform uni-lateral propagation of signals without a need of three-phase clock. This circuit is designed to use bridge-type Josephson junctions without hysteresis in their current-voltage characteristics, and is promising for high-speed logic device because of the small capacitances and high switching speed of 2 picoseconds, predicted by the computer simulation. An optimum circuit with maximum operating margin was found by varying design parameters such as the ratio of the critical current of Josephson junctions and inductances to get it as large as 50 % when the thermal noise at 4.2 K is considered. Three cascaded gates were modeled and simulated on a computer, and uni-laterality of signal flow was confirmed.


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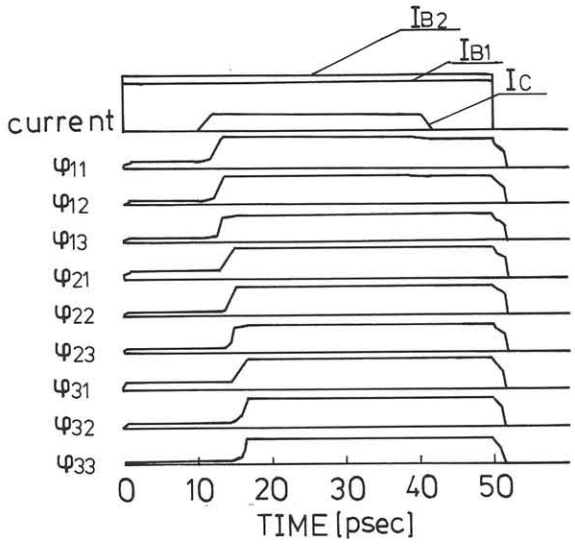


Fig.5 Simulated switching behavior of three cascaded gates, when $I_C$ is applied to the input junction of the first gate. The parameters are the same as in Fig.3.

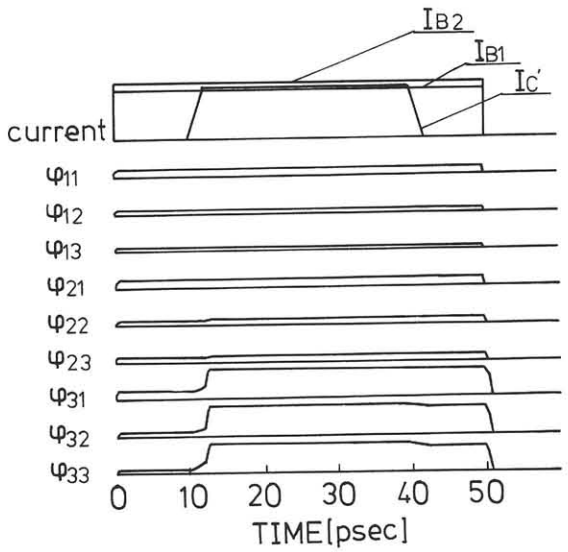


Fig.6 Simulated switching behavior of three cascaded gates, when $I_C'$ is applied to the output junction of the third gate. The parameters are the same as in Fig.5, except for $I_C'=2.1I_0$.

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