

Design and Characteristics of a 4 Mbits Magnetic Bubble Device

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Propagation patterns made by ion implantation make possible the fabrication of high density magnetic bubble memories by using conventional lithography processes. Good control of ion implantation into magnetic garnets as well as the implementation of new circuit designs are necessary in order to make operating devices. This paper shows the achievement of functions like nucleation, replication and detection and gives the performances of a 4 Mbits chip made by assembling these elementary functions.

§1. Introduction

This paper describes recent advances in the achievement of a 4 Mbits Magnetic bubble memory using ion implanted patterns for the fabrication of the propagator level. This technique makes possible the use of geometries larger than a micron ($\sim 1,2 \mu\text{m}$) on the different mask levels (propagation, conductor, detector) for the realization of a 4 Mbits bubble devices on a surface of 1 cm^2 . The main difficulty with this new technique is to be able to achieve special functions like swap gates and blok replicate gates that make possible the use of this 4 Mbits device with the existing L.S.I. support silicon circuits. This paper focuses on the achievement of these functions by using two different conductor levels and the performances of the 4 Mbits memory chips.

§2. Device fabrication

Devices are processed on $(\text{Y Sm Lu Ca})_3(\text{Fe Ge Si})_5 \text{O}_{12}$ bubble garnet with the following characteristics :

Thickness	$h = 1.2 \mu\text{m}$
Stripwidth	$W_s = 1.2 \mu\text{m}$
Collapse field	$H_c = 400 \text{ Oe}$
Characteristic length	$l = 0.13 \mu\text{m}$
Saturation Magnetization $4\pi M_s$	$= 800 \text{ G}$
Anisotropy field	$H_k = 1900 \text{ Oe}$

Wafers are first uniformly implanted with Ne ($50 \text{ keV } 1 \cdot 10^{14}$) and then through an implantation mask with hydrogen. The mask is made of 5000 \AA of gold on a 400 \AA chromium base deposited on 500 \AA SiO_2 . Implantation is performed through the SiO_2 at two energies (H_2 $90 \text{ keV } 4 \cdot 10^{16}$, $50 \text{ keV } 5 \cdot 10^{15}$). After removal of the gold and SiO_2 , wafers are annealed at 300°C for half an hour. The implantation results in an anisotropy field difference ΔH_k of 4000 Oe and a lattice deformation ($\Delta d/d$) of 1.15% . Then, insulating and conductive layers are deposited as shown on Fig.1. The two conductive layers (3000 \AA and 5000 \AA) are isolated by

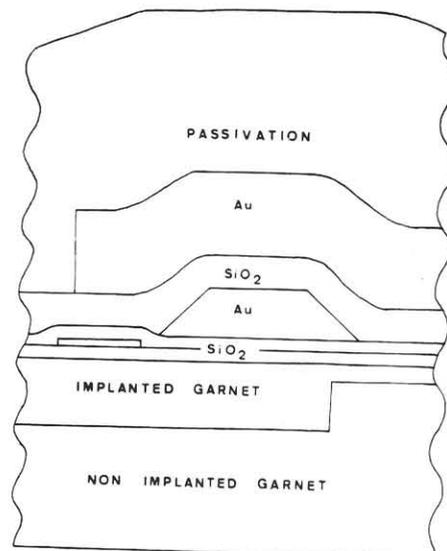


Fig.1

2000 Å of SiO₂. The stripe cutting conductor has been chosen to be in the first conductive layer because its low duty rate allows a reduced thickness. This conductor has its flanks ion milled at 45° in order to have good step coverage, this result is obtained with a thin photoresist mask (3000 Å) with a light thermal flow.

§3. Critical functions designs

1) Nucleation

This function is performed by the use of a hairpin loop located on the periphery of the propagation patterns as shown on Fig.2. The

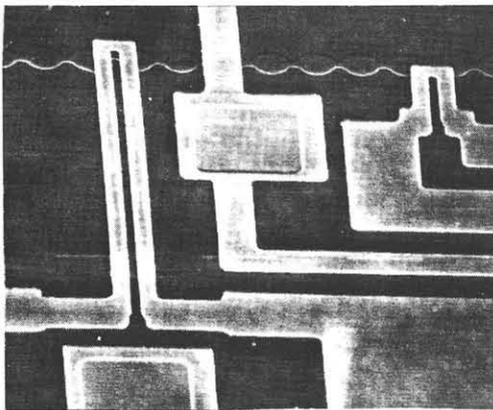


Fig. 2

margins in nucleate current as a function of the temperature are indicated on Fig. 3. The slope of this current is -0,6%/°C and the margins are + 20% of the nominal value.

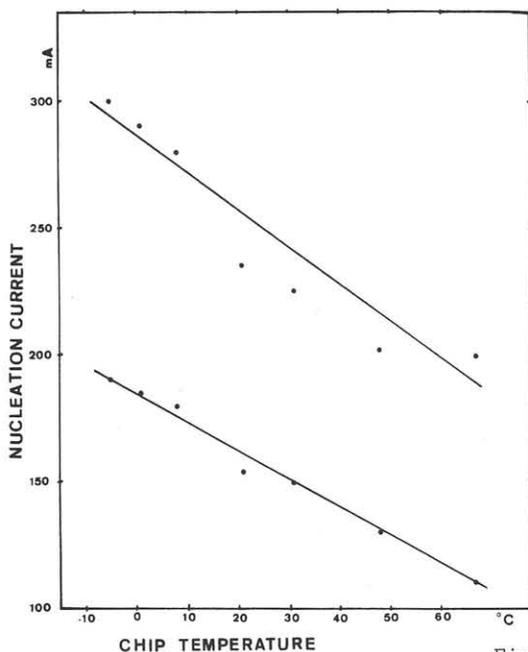


Fig. 3

2) Replication gate

The design of the replicate gate is shown on Fig.4. Replication is performed when bubble

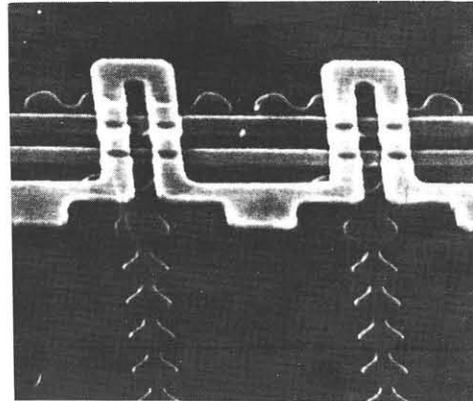


Fig. 4

are located at minor loop extremities in cusps to have good phase margins. Corresponding positions for replicated bubbles are located between two non adjacent non implanted patterns of the major loop to avoid bubble nucleation⁽⁴⁾ Bubble is first stretched between these locations and then kept stretched with a two level pulse in the stretching conductor. While the bubble is extended a short cutting pulse is applied with the first level conductor and bubbles are kept still in the cusps by a small current in the stretching conductor. Device is operated with a 55 Oe rotating field at 100 kHz Stretch current (160 mA) is applied during 300 ns and then half this current is maintained during a quarter of a cycle. Cut current (130mA)

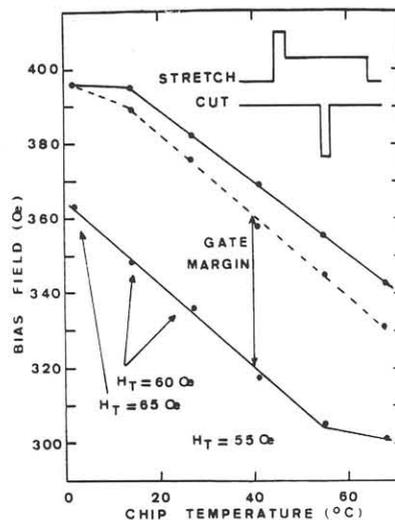


Fig. 5

is applied during 200 ns. Fig.5 shows bias field margins as a function of chip temperature for unmodified pulse conditions. The rotating field amplitude is larger at low temperature to maintain good propagation margins.

3) Detection

The detection station uses a long hairpin loop conductor for the extension of the bubble into a stripe domain ; A rectangular stripe of permalloy placed inside this loop detects the magnetic domain by its resistance change. A picture of the detector is shown on the left side of Fig.2. The conductor element is fed by two pulse currents, one for extension, the other for contraction. Bias field margins as a function of the chip temperature are shown on Fig.6. They are larger than 10% of the

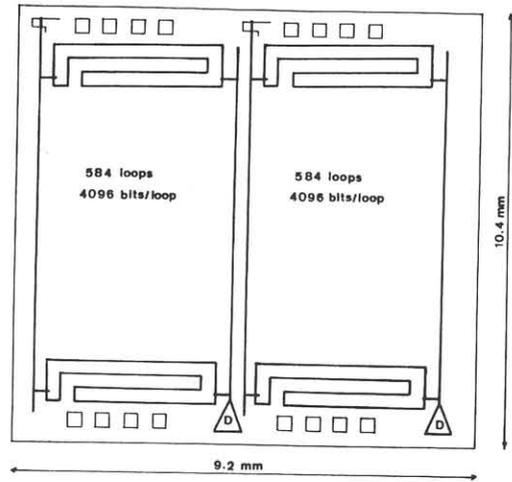


Fig. 7

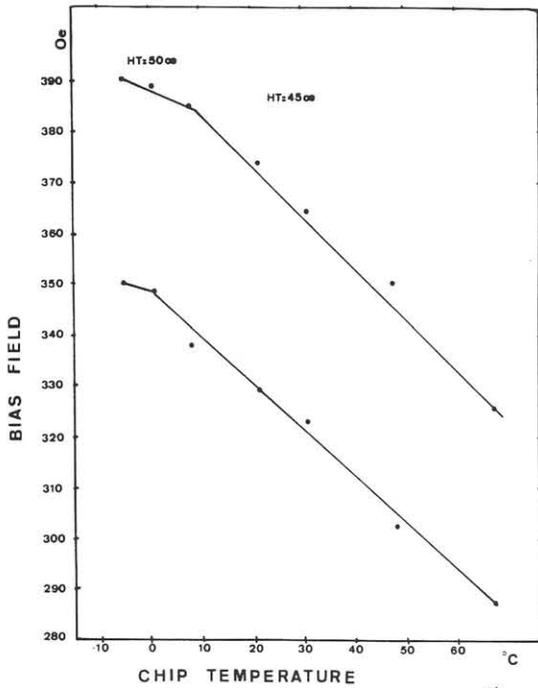


Fig. 6

mean value over the whole temperature range. The slope of the bias field variation fits the Baryum Ferrite magnet with the value of $-0,2\% ^\circ\text{C}$.

§ 4. Chip architecture and performance

The 4 Mbits chip is designed in order to be compatible with the controller fabricated for the 1 Mbits chip. It is constituted by 1168 loops having each 4096 bits (Fig.7), in order to decrease access time (20 ms) and increase data rate (200 kb/s) it is divided into two halves with two write and read stations. The overall dimensions of the component are 10,3 mm x 9,1 mm. This chip can be accommodated into the actual 1 Mbits bubble package.

