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HIGH PRECISION HALF-MICRON X-RAY MASK GENERATION BY E-BEAM LITHOGRAPHY

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In order to realize the next generation of VLSI and VHSIC(1), a half-micron geometry is needed. X-ray lithography would be one of the best choices for use in transfering half-micron patterns. Establishing X-ray mask fabrication is one of the key technologies in achieving X-ray lithography. Electron beam lithography is widely used in photolithographic mask fabrication(2). However, established resolution and pattern placement accuracy have not been sufficiently fine to allow fabricating X-ray masks. E-beam system for X-ray mask fabrication requires (a) half-micron resolution, (b) 0.05 um pattern placement accuracy, (c) very large scale and very high packing density pattern generating capability and (d) extremely low defect density. The authors reported electron beam lithography with a double layer resist process using silicon containing resist to obtain half- to quarter-micron resolution(3)(4). Silicon frames are usually used in X-ray masks, due to the ease in obtaining membranes (5). However, the pattern position accuracy on a conventionally fabricated X-ray mask using a silicon frame is worse than that of a photolithographic master mask that usually uses synthetic quartz. Since the thermal expansion coefficient of silicon is one order larger than that of synthetic quartz, the environmental temperature change easily affects X-ray mask substrate dimension, and temperature of electron beam work chamber must be carefully controlled. However, it is difficult to control temperature variations due to various causes, such as thermal emission from lenses and stage driving motors. One solution is using placement alignment marks on masks similar to electron beam direct writing methods(6). However, this results in defect density increase and throughput decrease due to the excess process steps. Defects are fatal in a step-and-repeat X-ray exposure system(7) which matches ever-enlarging wafers. This paper describes processes to fabricate high precision X-ray masks with low-defect large-scale half-micron patterns.

Figure 1 shows the X-ray mask fabrication steps. Double layer resist, consisting of 0.2 um thick dimethylsiloxane and 1.6 um thick buffer layer, was spin-coated on thin gold/SiN_x/Si substrate. The thin gold was for thick gold electroplating and the plasma enhanced CVD SiN_x was for membrane(8).

The electron beam exposure system used to fabricate X-ray masks was a variable shaped beam vector scan machine that was able to generate very large scale and very high density patterns with high throughput(9). The accelerating voltage was 20 kV and the current density was 0.4 A/cm^2. Figure 2 shows the cassette used in e-beam exposure. The cassette has a silicon ring with four orthogonally located fiducial marks. An X-ray mask substrate is placed at the center of the cassette so that mask center and ring center coincide. When a mask is affected by thermal expansion, the ring of the same silicon also has the proportionally same amount of thermal expansion. As shown in Fig. 3, pattern positions were corrected similar to the direct writing method by detecting the positons of marks on the ring and correcting writing position errors due to expansion and beam drift. However, the mark position detection accuracy is better than direct writing, because there is no resist coating on the marks.

Pattern placement accuracy on a mask was measured by an automated electrical measurement technique(10), that has high throughput and high measurement accuracy of 0.005 um. Figure 4 shows the method utilized for determining pattern placement accuracy in this work. Van der Pauw resistors are located on the center and the four corners of a test chip which is the same size as electron beam deflection field. The test chip is composed of two exposure levels and applicable for (1) overlay accuracy measurement and (2) field stitching accuracy measurement. For (1), the second level is exposed coinciding the chip center, and for (2), the second level is exposed with a shift to overlap the corner.

Figure 5 shows pattern overlay misalignments between two pattern levels, achieved by this system and a conventional system. Pattern placement accuracy obtained by the convetional system is $\pm$ 0.08 um, which does not satisfy the requirement. On the other hand, the values achieved by this system are within $\pm$ 0.04 um, which satisfies the requirement.

Figure 6 shows an X-ray mask pattern generation steps of shrinked 512k ROM(11),an example of an X-ray mask fabricated using high-resolution double layer resist and this noble thermal-expansion-correction method. Half-micron wide patterns were easily achieved with high precision.

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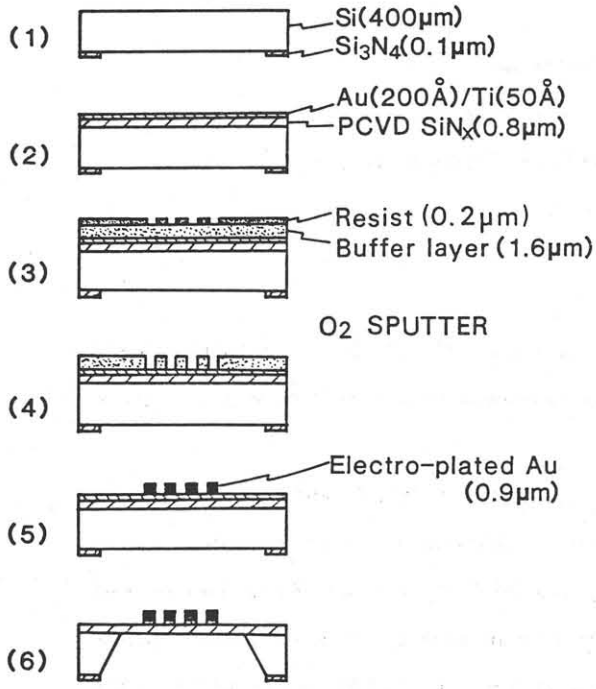

Fig. 1 X-ray mask fabrication steps.

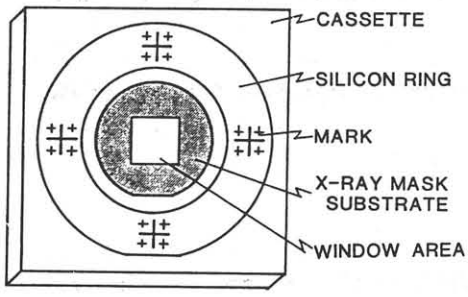

Fig. 2 New cassette with Si ring.

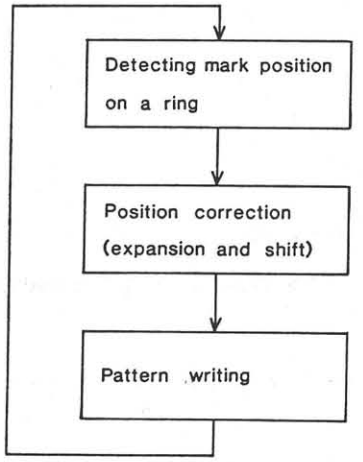

Fig. 3 Thermal-expansion-correction flow chart.

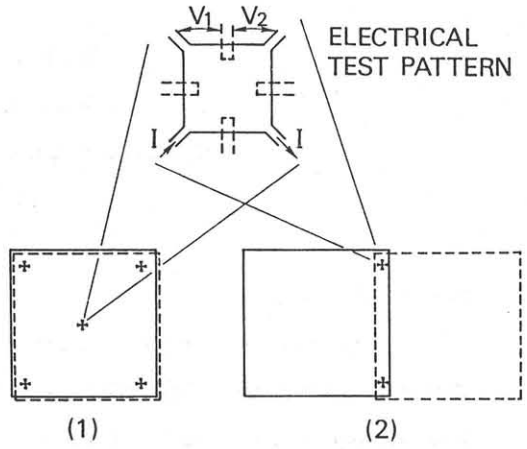

Fig. 4 Method determining (1) overlay accuracy and (2) field stitching accuracy. Solid lines and dotted lines show the first and the second level respectively.

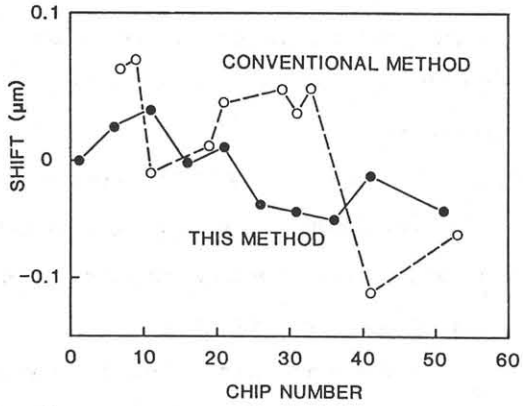

Fig. 5 Pattern placement accuracy comparison between this system and a conventional system.

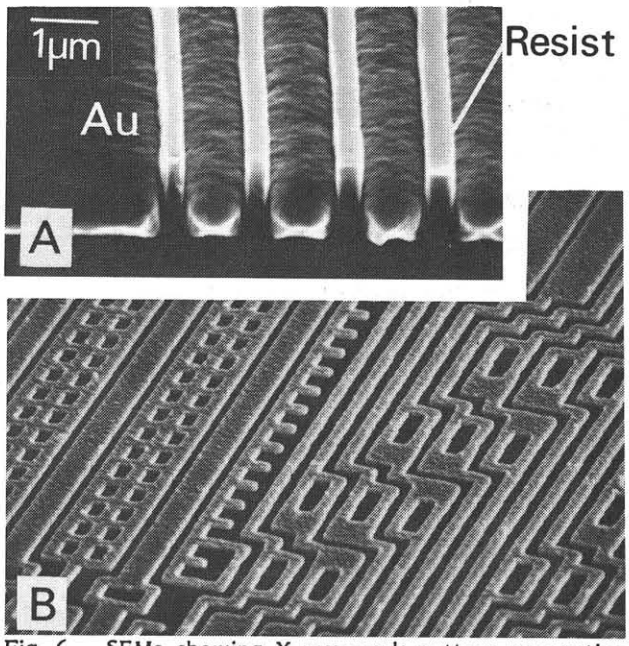

Fig. 6 SEMs showing X-ray mask pattern generation process.
(A) Electro-plated Au pattern with double layer resist pattern.
(B) After removal of resist pattern.