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Transient Analysis of Drain Current in Silicon-On-Insulator (SOI) MOSFET's

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Compared with conventional transistors, SOI MOSFET's show incompatible electrical characteristics due to substrate-floating effect. A remarkable feature of SOI device characteristics is observed in switching waveforms in digital circuits. In order to explain the switching characteristics and to understand frequency dependent propagation delay, a charge pumping model was proposed. The model predicts that, after turning on a MOSFET, drain current overshoot characteristic caused by minority carriers is observed in the time range of 100 μsec. Our transient analysis of MOSFET, however, proves that majority carriers , instead of the minority carriers, in the floating substrate strongly affect the current overshoot. In this paper, we present a new model for the switching characteristics of SOI MOSFET.

An MOSFET having channel length of 2 μm is fabricated on SOI substrate in a standard process line. Gate oxide and SOI film thicknesses are 70 nm and 1 μm, respectively. Experimental switching waveforms are shown in Fig.2. The turn-on drain current overshoots up to more than twice of a steady-state value, and then decreases to a steady-state value in about 200 μsec. A comparison between Figs.2(a) and 2(b) indicates that the current overshoot increases with "off" time interval up to about 1 msec.

We developed a rigorous 2-carrier and transient SOI device simulator to analyze the switching characteristics. Fig.3 shows the simulated drain current which agrees with the experimental results. On the analogy of substrate bias effect, after turning on the MOSFET, excess majority carriers (holes for n-channel transistors) flow into the floating substrate, which raises the substrate potential and results in the increase of the drain current. Then, the drain current decreases to the steady-state value until the excess majority carriers recombine completely with minority carriers. Inset of Fig.3 shows that, in the time range of 10^{-10} to 10^{-7} sec, the turn-on current remains almost constant because recombination of majority carriers is negligibly small. It should be, however, noted that the current overshoot characteristic is a strong function of the floating substrate potential just before the transistor is switched from the "off" state to the "on" state.

Inset of Fig.4 shows a substrate potential during the "off" state of the SOI MOSFET, in which two distinct potential increases are observed. The potential increase in the short time range (10^{-12} to 10^{-10} sec.) is caused by the minority carriers (electrons) flowing into the source and the drain regions, while the one in the long time range (10^{-4} to 10^{-3} sec.) is caused by thermally generated majority carriers (holes). Note that a subsequent pulse applied to a non-equilibrium state MOSFET significantly reduces the overshoot of the drain current as shown in Fig.2(a).

The utilization of our simulation techniques allows us to clarify the mechanism of digital operation in SOI MOSFET's.

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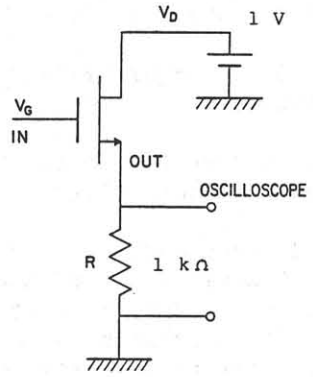
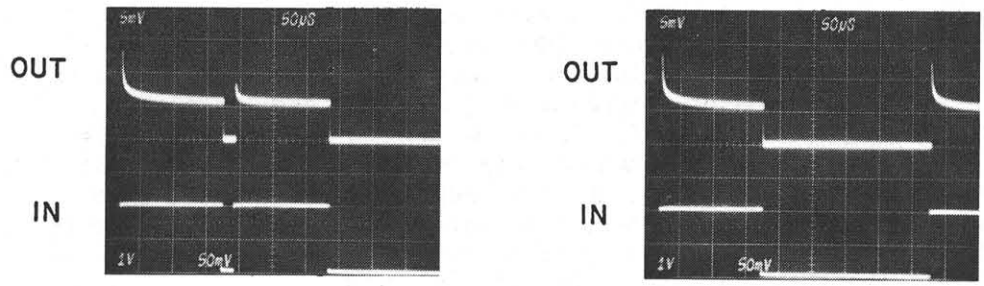


Fig.1 Circuit to measure switching characteristics of drain current.



(a) (b)

Fig.2 Observed switching characteristics when the sequential gate pulses of 2 V are applied with (a) an interval of 20 μs and (b) an interval of 250 μs.

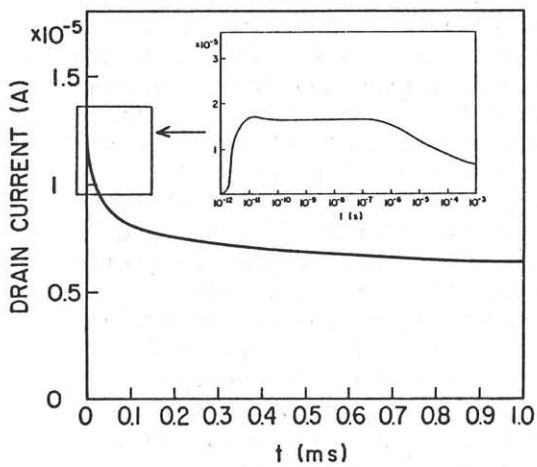


Fig.3 Simulated turn-on characteristic when the gate voltage is increased. Life time is assumed to be 10 ns for both electrons and holes.

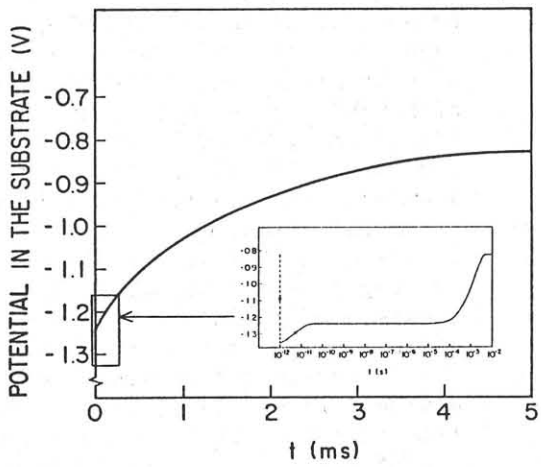


Fig.4 Simulated time dependence of the substrate potential when the gate voltage is turned off. Life time is assumed to be 10 ns for both electrons and holes.