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SOI / CMOS Gate Array by Laser Recrystallization

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This paper describes 440-gate CMOS Gate Arrays fabricated by a laser recrystallized SOI (Silicon on Insulator) technology for the first time.

Recently, many investigations for SOI devices and techniques have been performed. Especially laser recrystallization is paid much attention as one of the most effective techniques for the realization of SOI/IC's[1,2]. The realization of SOI/IC's is expected because of their characteristics of high speed and latch-up free etc. While some 3-D circuits as ring oscillators[3] and shift registers[4] have been fabricated as test devices, none has been called the integrated circuits indeed. It is difficult to make device-worthy silicon films on amorphous insulating layers with good reproducibility. Poor reproducibility causes poor yield of devices in a chip. However, by several improvements of annealing techniques and equipments, we can obtain bearable crystalline islands with good yield now. Then we succeeded in fabricating of SOI/IC's——440-gate SOI/CMOS Gate Arrays.

The Gate Array has 440 fundamental elements named Basic Cell (BC). A BC consists of two pairs of p-channel and n-channel MOSFET's with $L = 2.8$ µm and $W = 30$ µm. Fig.1 shows a pattern and an equivalent circuit of a BC. The BC's are set in array of 55 rows and 8 columns. In periphery of the array of BC's, I/O cells are laid.

The fabrication process is as follows. A 0.4 µm thick layer of polysilicon over a thermally oxidized silicon film was recrystallized by using laser beam irradiation. We use some kinds of laser recrystallization techniques as the heat-sink method etc.[5,6] During the recrystallization, the scanning cw argon ion laser beam was used with a power of 5-10 W. The silicon islands for p-channel and n-channel MOSFET's were doped by ion implantation with arsenic ($2x10^{11}cm^{-2}$, 80 keV) or boron ($2x10^{11}cm^{-2}$, 120 keV), respectively. A 400 nm thick layer of gate oxide was grown by thermal oxidation. After the formation of polysilicon gate electrodes (0.4 µm thick), source and drain regions of MOSFET's were implanted with boron ($1x10^{15}cm^{-2}$, 35 keV) or arsenic ($3x10^{15}cm^{-2}$, 120 keV). Then the wafers were annealed at 900°C nitrogen atmosphere for 40 minutes. Wiring was performed by using 2-level aluminum metallization technique. A finished sample is shown in Fig.2.

In this experiment, the circuits of ring oscillators (7-stage and 15-stage) and frequency dividers which have different stages (largest: 12-stage) were customized. Each stage of the frequency dividers consists of 10 BC's (i.e. 40 MOSFET's). Threfore, a 12-stage frequency divider has more than 480 MOSFET's, including I/O cells. Fig.3 and Fig.4 show output waveforms of a ring oscillator and a frequency divider, respectively. Fig.3 illustrates that the propagation delay time is 530 psec a stage at 8.0 V of power supply. This value is about 70% of that of a conventional Gate Array made on a single crystal silicon substrate. Threshold voltages are from -1.2 to -0.5 V for the

p-channel MOSFET's and from 0.5 to 1.2 V for the n-channel MOSFET's. Field effect mobilities are about 130 $cm^2 \cdot V^{-1} \cdot sec^{-1}$ for the p-channel MOSFET's and about 530 $cm^2 \cdot V^{-1} \cdot sec^{-1}$ for the n-channel ones. These values will be improved, as process conditions are improved.

By this attempt, we have good perspective of SOI technology application to IC's.

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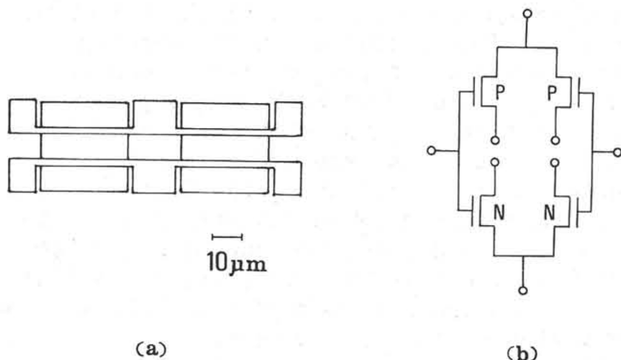

Fig.1 Basic Cell
(a) Pattern (b) Equivalent Circuit

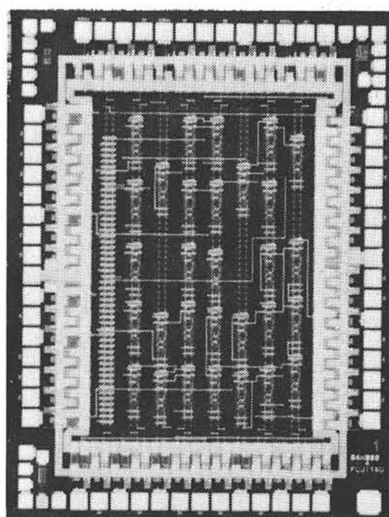

Fig.2 440-gate SOI/CMOS Gate Array

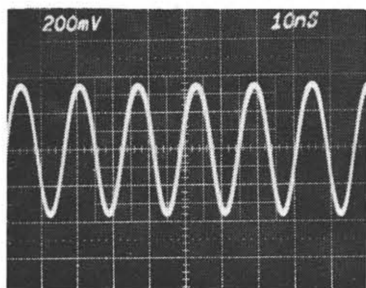

Fig.3 Output waveform of a 15-stage ring oscillator (V_{DD} = 8.0 V , L = 2.8 μm)

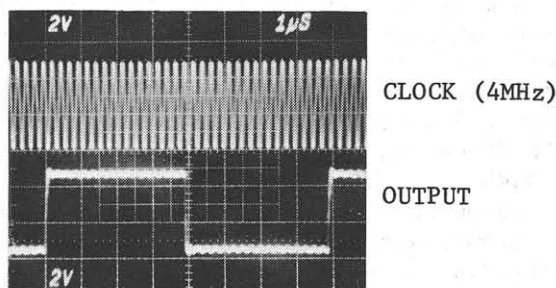

Fig.4 Output waveform of a 5-stage frequency divider (Clock Frequency : 4 MHz , V_{DD} = 5.0 V)