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Three-Dimensional SRAM-Cell Fabricated with a Laser-Recrystallization Technology

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Exploratory SRAM cells have been fabricated with a three-dimensional (3-D) CMOS-IC technology,[1] where an n-channel SOI-MOSFET is fabricated directly above another p-channel bulk-MOSFET insulator in between, for the first time. The memory cell contains 5 MOSFET's. A flip-flop of the memory cell consists of two 3-D inverters and a transfer gate consists of a n-channel SOI-MOSFET placed in the vicinity of the flip-flop. Figure 1 shows the fabricated test circuit. The sense amplifier is also formed with a 3-D inverter.

Fabrication of this 3-D memory starts with an n-type, (100) 10 Ω cm silicon wafer. A 0.6 μm field oxide is thermally grown by the LOCOS technique. A 500 Å gate oxide is formed and a 0.4 μm polysilicon is deposited and patterned. The source and drain region of the bottom devices are made with boron implantation at 40 keV to 1×10^{15} cm^{-2}. A 0.6 μm phospho-silicate-glass (PSG) is deposited and reflowed at 1050 °C. At this reflow step, the gate polysilicon of the bottom p-channel bulk-MOSFET's is doped n^+ type by phosphorus diffusion from the PSG film. Then a 500 Å Si_3N_4 is deposited to prevent phosphorus diffusion to the recrystallized silicon. This double-layer of Si_3N_4 and PSG is used as an intermediate insulating layer between the top and bottom devices. A 0.4 μm polysilicon is deposited and recrystallized by cw argon laser irradiation with a 10 W power, a 38 mm/s scanning speed at 450 °C in air. The device region of the top MOSFET is defined by etching the recrystallized silicon. A 480 Å gate oxide is thermally grown. A 0.4 μm polysilicon is deposited and defined for the gate electrode of the top devices. Source and drain regions are formed by arsenic implantation at 150 keV to 3×10^{15} cm^{-2}. Contact holes for the bottom devices are opened and a 500 Å oxide is thermally grown in the holes. A 0.5 μm PSG is deposited and contact holes are opened again simultaneously for both the top and bottom MOSFET's. The top and bottom devices are directly connected by wiring of 1.0 μm aluminum.

Figure 2 shows the 3-D CMOS RAM cell in the test circuit shown in Fig.1. Channel lengths are 6 μm for all the MOSFET's. Field effect mobilities are 350 $cm^2/V \cdot s$ for the n-channel bulk-MOSFET's and 250 $cm^2/V \cdot s$ for the p-channel SOI-MOSFET's. Threshold voltages are 0.5 V for the n-channel devices and -1.1 V for the p-channel devices.

Figure 3 and 4 confirm the function of the RAM cell. Figure 3 shows that information '1' is written in the memory cell and this information is read out. WRITE '1' operation is performed by applying 5 V to the WRITE ENABLE, DATA INPUT, and WORD lines. During this time, the OUTPUT voltage is low because the bit line is kept at high voltage. By applying 0 V to the WORD line, the transfer gate is turned off. In the memory cell, a information '1' is stored. The stored information is confirmed as follows. The bit line is pre-charged to 0 V by applying 5 V to the WRITE ENABLE while the DATA INPUT is kept at 0 V. After the WRITE ENABLE is biased to low, the transfer gate is turned on, by applying 5 V to the WORD. The bit line is charged up to 5 V due to the stored '1' information, and the OUTPUT voltage of 0 V is obtained.

Figure 4 shows that information '0' is written in the memory cell and this information is read out. At first, the operation of WRITE '0' is performed by applying 5 V to the WORD and WRITE ENABLE lines while the DATA INPUT is kept at 0 V. After the transfer gate is turned off, the bit line is pre-charged to 5 V by applying 5 V to the WORD and DATA INPUT lines. When the transfer gate is turned on while the WRITE ENABLE is kept at 0 V, a high voltage is obtained for the OUTOUT. This means that the information '0' stored in the cell is read out.

REFERENCES

1) N. Sasaki et al., the 15th Conf. Solid State Devices and Materials, Tokyo, 1983, Late News A-3-7LN, Suppl. Extended Abstract p.24.

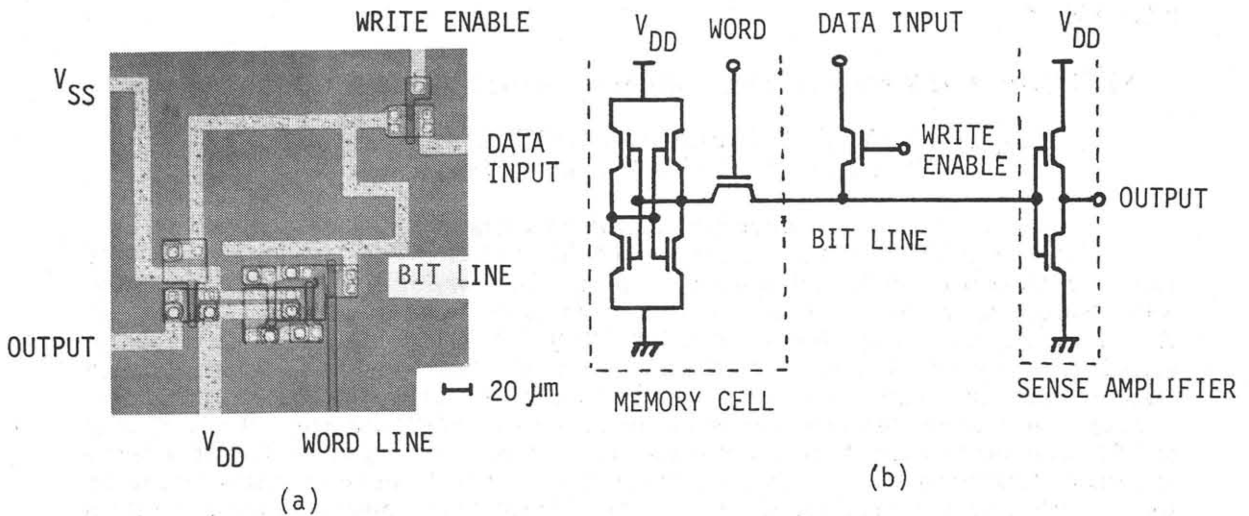

Fig.1. Test circuit of the 3-D SRAM cell.
(a) Photomicrograph and (b) equivalent circuit.

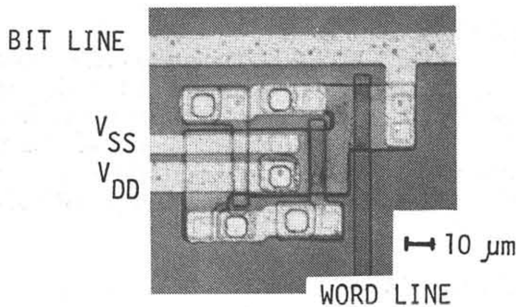

Fig.2. 3-D SRAM cell.

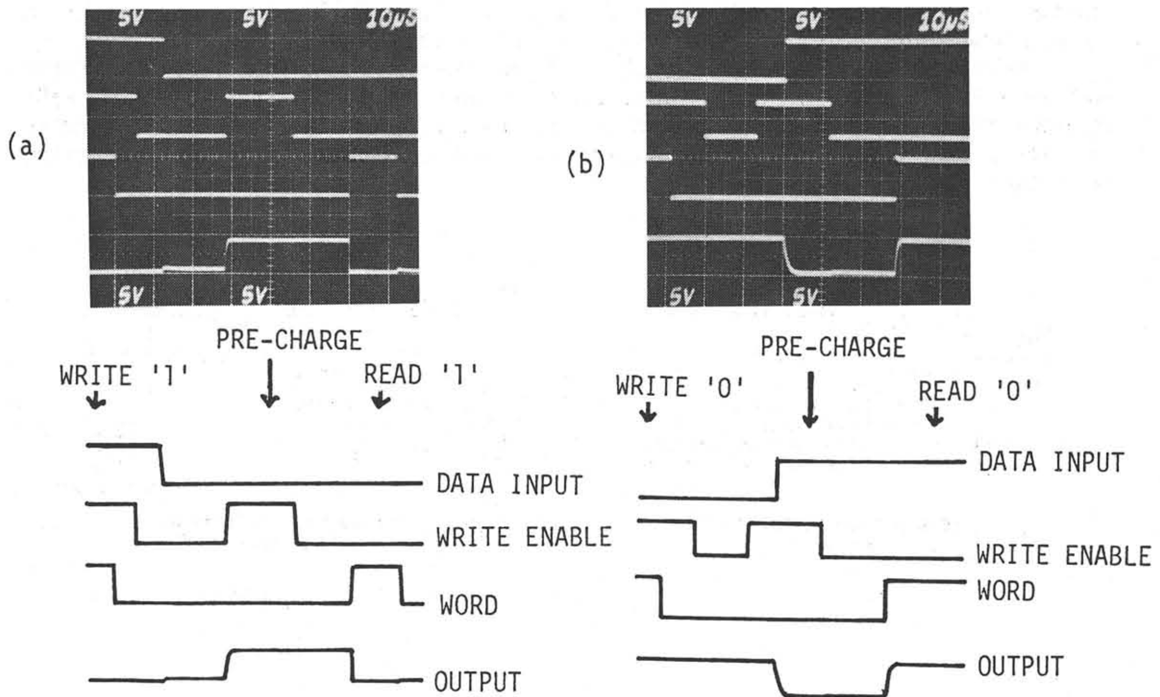

Fig.3. Waveforms for the memory operations of 3-D SRAM cell.
(a) WRITE '1' and READ '1' and (b) WRITE '0' and READ '0'.