LC-12-7

VLSI-Oriented Voltage Down Converter with Sub-Main Configuration

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I. Introduction and Basic Ideas

Submicron VLSI's suffer from reliability degradation due to high electric field effects, such as breakdown, substrate current, and hot carrier problems. Consequently, lower voltage operation is necessary while maintaining external power supply of 5V. Therefore, on-chip Voltage Down Converter (VDC) is of great importance for realizing scaled down devices. However, no attempt has been made to build a VDC which has a standby mode (extremely low power state) and enables battery backup of the device, although this standby feature is indispensable for static RAM's and logic VLSI's, since it is difficult to cover both of the standby and active mode by using one VDC. We propose sub-main structured VDC to solve this problem. A sub VDC which is characterized by its very low power dissipation and low current drivability is placed in parallel with a main VDC which has high current drivability and medium power consumption, as shown in Fig.1. When a chip enable signal (CE) goes low, the main VDC is disabled and only the sub VDC is active to supply leak current of several micro-amperes for data storage of memories and registers. This type of sub VDC can be constructed with power dissipation less than a micro-ampere, which is tolerable for battery backup use.

II. Test-Chip Results

Figure 2 shows the circuit diagram of the VDC. High resistive elements are used to realize low power standby operation. The high resistive element in the V_{ref} generator helps to achieve fast recovery from the standby. Photomicrograph of the test-chip is shown in Fig. 3 and the circuit area is 0.1 mm^2 using 2μm design rule. Satisfactory results are obtained for output characteristics and load characteristics, as shown in Figs.4 and 5, respectively. Figure 6 is simulated transient waveforms of voltage and current for active and standby mode.

III. Considerations

To clarify the appropriate way to apply low voltages to static memory cells, V_{DS}-V_{GS} trajectories are calculated as in Figs.7. Read "0" operation is dangerous in terms of the reliability. Low bit line voltage mitigates the gate current by an order of one per one volt down, without degrading bit line delay (Fig. 8 and 9). Word line voltage should not be lowered since it much deteriorates the access time.

As for the VDC design, relationship between feedback loop delay (τ_f) and ripple voltage of the internal V_{DD} are estimated by a simple model. The result (Fig.10) tells that the τ_f should be chosen sufficiently small compared with a feed forward delay (RC) for stable operation. Feedback gain consideration is also discussed using more generalized model.

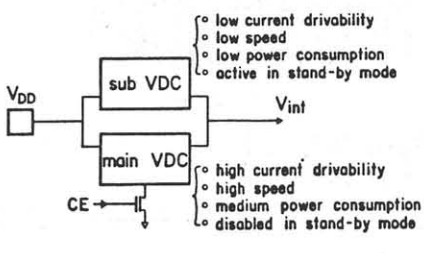


Fig.1 Basic configuration of proposed VDC.

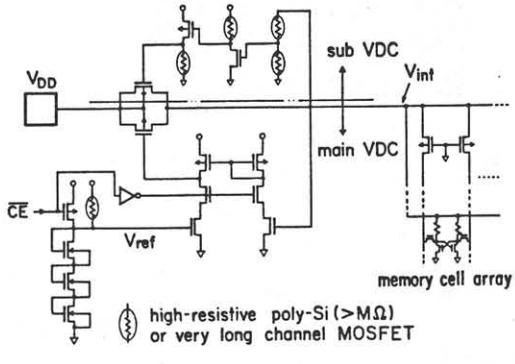


Fig.2 Circuit diagram.

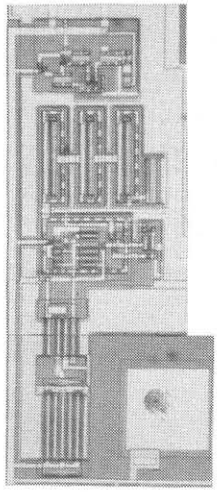


Fig.3 Photomicrograph of the test-chip.

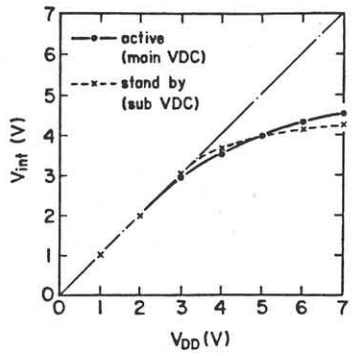


Fig.4 Measured output characteristics.

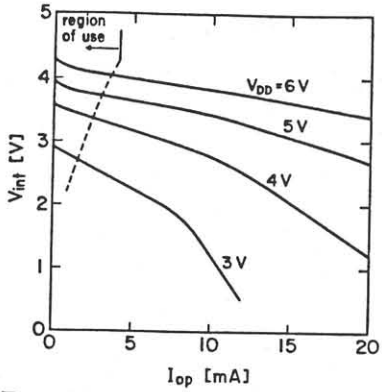
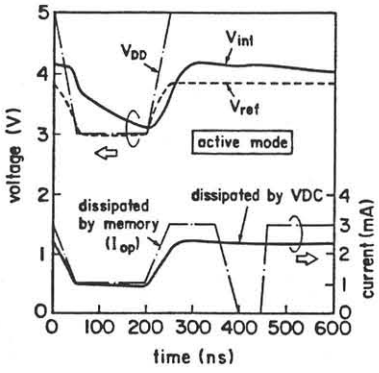


Fig.5 Measured current supply characteristics.



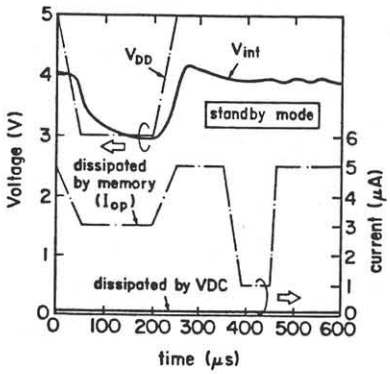
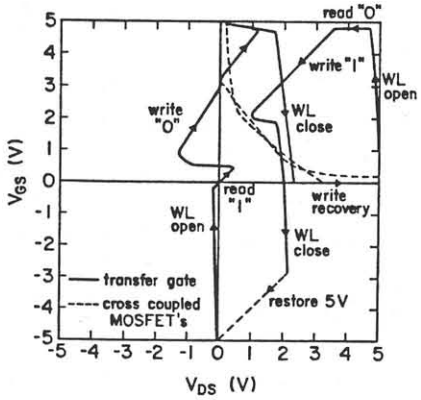


Fig.6 Simulated waveforms of the VDC.
(a) active mode, (b) standby mode.



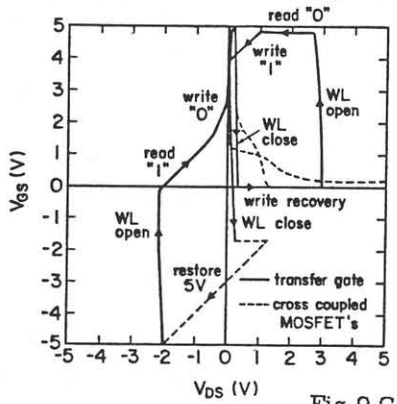


Fig.7 V_{DS}-V_{GS} trajectory of static RAM cell with (a) 5V bit line, (b) 3V bit line.

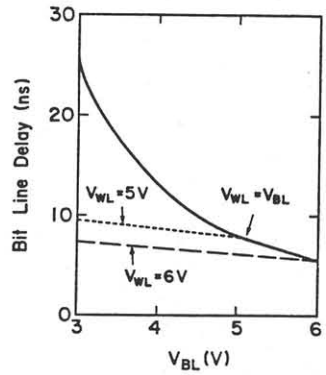


Fig.9 Calculated bit line delay with various bit line voltage.

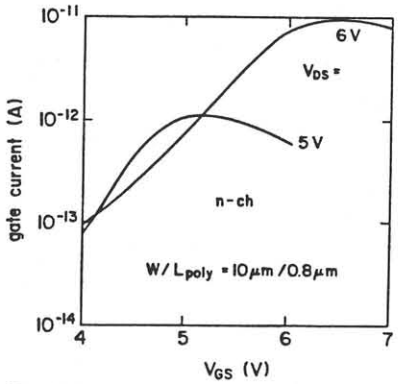


Fig.8 Measured gate current for submicron MOSFET.

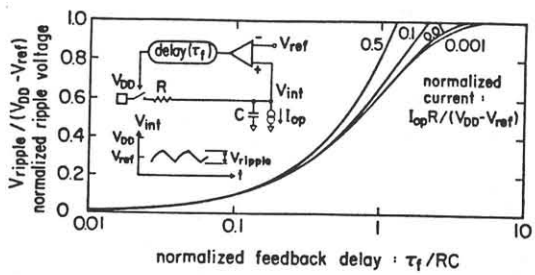


Fig.10 Ripple voltage vs. feedback delay.