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Planar GaAlAs/GaAs Heterojunction Bipolar Transistors

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Heterojunction bipolar transistors (HJBTs) are very promising for high speed applications. Their high cutoff frequency and high speed performance have been demonstrated using MBE grown GaAlAs/GaAs heterostructures.[1-3]

In spite of these encouraging results, there still remain problems to be solved. Especially, a planar structure suitable for higher grade of integration has not been realized for HJBTs. In order to fabricate the planar structure out of MBE or MOCVD grown layers, three basic processes are required: (1)isolating devices from each other, (2) forming contacts to the base layer beneath the surface, and (3) forming contacts to the collector layer. Processes (1) and (2) have been successfully performed by ion implantation,[2] thereby maintaining a flat surface necessary for the fabrication of planar HJBTs. However, regarding process (3) it is difficult to obtain planarized collector contacts using similar technology, because it seems almost impossible to change the conduction type of heavily doped p^+ base layer existing above the collector layer into n^+ type by a compensating diffusion or ion implantation. In previous works, mesa etching was adopted to form contacts to the buried collector.[1-3]

This work describes a new planar structure heterojunction bipolar transistor that is suitable for high density integration. The key technology of the planar structure are (a) reactive ion etching (RIE) followed by (b) metal re-filling to provide a direct contact to the buried collector layer from the wafer surface, and (c) ion implantation to isolate the contact sidewall from the extrinsic base region.

Figure 1 shows an SEM micrograph of the fabricated collector contact. Boron ion implantation is carried out to provide an intra-device isolation region between base and collector contacts. Recessing the contact holes is carried out by RIE, wherein a nearly vertical GaAlAs/GaAs etching profile is achieved by using BCl_3/Cl_2 mixed gas.[4] Ohmic metal of AuGe/Au is evaporated to re-fill the holes and is lifted off by the photoresist used as an etching mask.

The HJBTs are fabricated out of MBE grown wafers, whose layer constitution is presented in Table 1. Figure 2 illustrates the structure of the fabricated HJBTs. Device fabrication processes start with selective magnesium ion implantation followed by infrared lamp annealing, to form the p^+ contact region to the base layer from the surface, which simultaneously defines the emitter area. Both intra- and inter-device isolation are provided by boron ion implantation. Collector contacts are obtained using the processes previously described regarding Fig.1. After forming emitter and base contacts, shallow boron implantation is carried out to eliminate the parasitic homo p-n junction existing in the GaAs cap layer. Interconnection is formed by using Ti/Pt/Au.

Figure 3 shows the I-V characteristics of a 5 μm x 50 μm emitter size device. Current gain of 30 is obtained at current density of 10^4 A/cm^2. This value is comparable to that of the devices fabricated by a conventional mesa etching process.

In conclusion, a new planar structure is proposed for HJBTs with successful results. Although collector contact areas are relatively large in this work, e.g. 10 μm x 50 μm, it seems easy to reduce the size down to 2 μm or less. This

technology is promising for larger scale integration of HJBT.

Acknowledgement

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References

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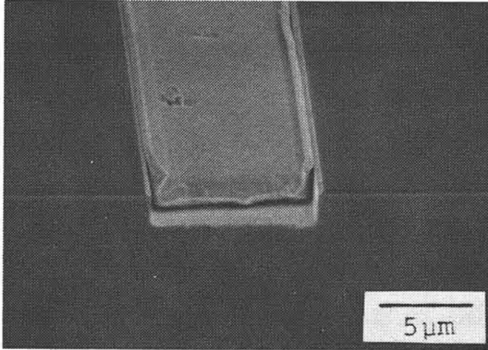

Fig.1 SEM micrograph of a metal filled collector contact.

Layer		Thickness (Å)	Doping (cm^{-3})	
Cap	n^+GaAs	1000	2E18	
	n GaAs	1500	3E17	
Emitter	n $Al_xGa_{1-x}AS$	500	3E17	E_g grading
	n $Al_{0.3}Ga_{0.7}As$	1000	3E17	
	n $Al_xGa_{1-x}As$	500	3E17	E_g grading
Base	p^+GaAs	1000	3E18	
Collector	n GaAs	5000	5E16	
	n^+GaAs	3000	2E18	
Substrate	SI GaAs			

Table 1 MBE layer structure

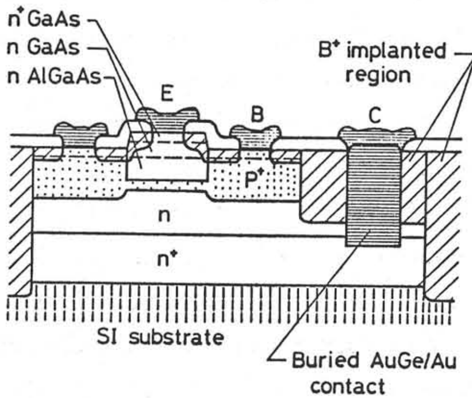

Fig.2 Cross section of a planar structure heterojunction bipolar transistor.

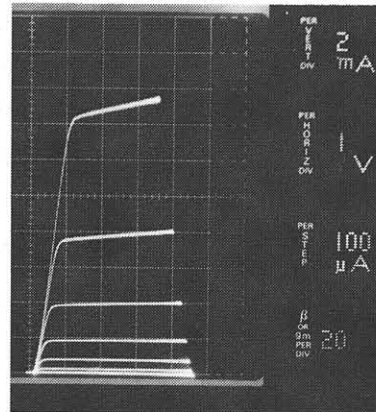

Fig.3 Common emitter output characteristics of a planar HJBT.