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GaAs DFET Logic operated on Single Supply Voltage

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GaAs depletion mode MESFET logics (DFET logics), such as BFL or SDFL, have a larger noise margin in comparison with DCFL. However, they require a negative supply voltage in order to switch depletion mode FETs. C^2L (Capacitor Coupled Logic(1)) does not need the negative supply voltage in spite of the DFET logic. However, it does not operate at the low frequency region and it is necessary to initialize the logic condition.

This paper describes a DFET logic operated on a single supply voltage, which operates from DC to GHz region. Figure 1 shows current flow for an inverter chain circuit. It has a common source line called a virtual grounded line and a voltage stabilizing diode DG. When Q_1 DFET gate voltage is low, Q_1 is off and load current I_{L1} flows to Q_2 gate through a level shift diode D_{L1}. The current $(I_{L1} - I_{S1})$ goes into Q_2 FET, because of the Schottky gate structure. At that time, Q_2 is on and drain current $(I_{L2} - I_{S2})$ goes to the Q_2 source. Therefore, diode current I_{DG} is two times $(I_L - I_S)$, when I_{L1} equals I_{L2}, and I_{S1} equals I_{S2}. If an N stage inverter chain exists, diode current I_{DG} becomes N times $(I_L - I_S)$, whether FET gate voltage is low or high. Therefore, I_{DG} is kept at a constant value, and it supplies a constant voltage for the virtual grounded line. Moreover, the voltage stabilizing diode reduces voltage variation of the virtual grounded line at the inverter transition periods, since diode voltage is proportioned to a natural logarithm of it's current. Eventually, the virtual grounded line operates as a ground, whose voltage is lifted as the diode DG voltage from an actual ground line, and the logic can operate without a negative supply voltage. This logic is called VGL (Virtual Grounded Logic).

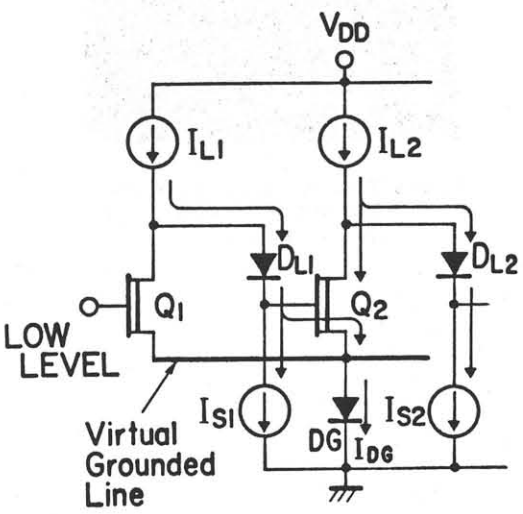


Figure 1

Saturated resistors (2) are used for current source I_L and current sink I_S in order to improve operational speed by eliminating gate capacitances, because of their very small junction capacitance value compared with that of FET load.
The fabrication process used for the logic is a Pt buried gate FET process (3) with 1 μm gate length on masks.

Figure 2 shows propagation delay time as a function of power dissipation per gate in a ring oscillator. About 45 psec propagation delay time is achieved at 15 mW power dissipation per gate. Less than 60 psec propagation delay time is expected at a few mW per gate from the data shown in Fig. 2. Figure 3 shows a T-type master-slave flip-flop circuit (A) and basic cell (B). Saturated resistors SR_1 and SR_2 were also used.

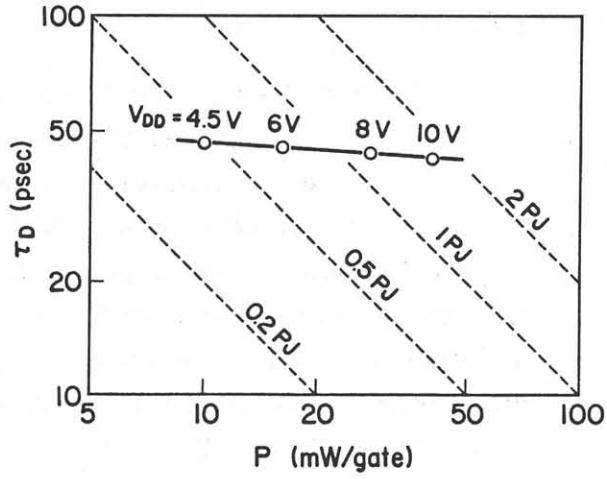
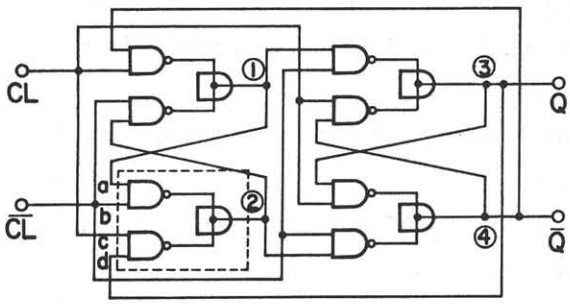
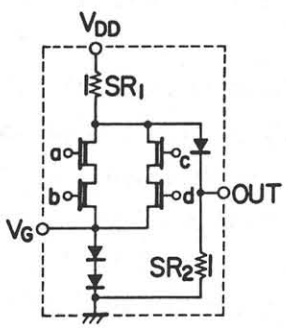


Figure 2

Figure 4 shows a divide by four flip-flop operation at low frequency region. Upper and middle waveforms are input signal and output signal, respectively. Lower waveform is about 1.75 V virtual grounded line voltage. Maximum toggle frequency was 1.72 GHz at 50 mW per flip-flop.



(A)



(B)

Figure 3

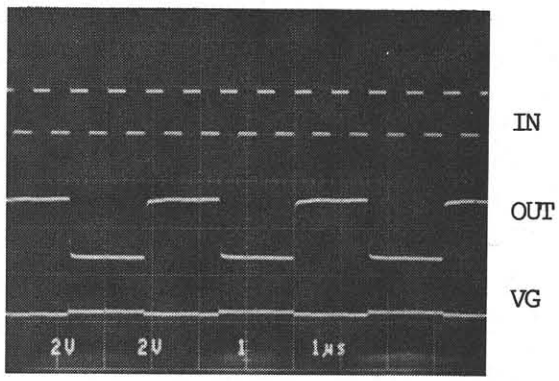


Figure 4

Acknowlegment

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References

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