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A 2 ns GaAs 4kb SRAM Using a Dislocation Free LEC Crystal

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Full operation of high speed GaAs SRAM's which consist of DCFL circuits is attainable by reducing scattering of the threshold voltage. According to our circuit simulation, full operation is obtained in case of threshold voltage standard deviation of less than 30 mV, at V_{TE} = 0.15 V for E-FET and V_{TD} = -0.4 V for D-FET.

We applied dislocation free wafers to 1 um gate-length SAINT process in order to reduce the scattering. The wafers were In-doped, semi-insulating, (100), LEC-grown GaAs. The etch pit density of 0 to 200 cm^{-2} was measured by counting the etch pits revealed with molten KOH, excluding the wafer periphery.

A 10:1 projection mask aligner was used in order to improve the gate length uniformity.

A circuit configuration of 1kW x 4b SRAM is improved to be insensitive to scattering and shift of the threshold voltage. Source-followers are used for driving the word-lines, to switch transfer-gate FETs on/off without failure. Complementary outputs from the sense amplifier are fed to the output buffer amplifier instead of the conventional push-pull type outputs.

The fabricated wafer had the average threshold voltage of 0.297 V for E-FET and -0.266 V for D-FET. Threshold voltage standard deviation for E-FET was 17 mV in the 2 inch wafer. The microphotograph in Fig.1 shows a completed 4kb SRAM chip. Chip size is 4.3 mm x 3.6 mm.

The histogram for pass bit number per chip is shown for 16 chips fabricated in the 2 inch wafer in Fig.2. Fail bit testing was performed with a marching pattern by a memory tester. We obtained, for the first time, a fully operated 4kb SRAM. The second best chip had pass bits of 4090. The histogram for address access time in the fully operated chip is shown in Fig. 3. This was also measured with the memory tester. Minimum access time was 4 ns and maximum one was 16 ns with 490 mW power dissipation at V_{cell} = 1.5 V and $V_{periphery}$ = 1.0 V. Typical access time was 7 ns. The best minimum access time in another chip was 2 ns with 539 mW. The access time difference between the measured value of

2 ns and the calculated value of 1.4 ns is due to disagreement of the threshold voltage between the fabricated value and the designed value.

In conclusion, a fully operated, practically applicable, GaAs 4kb SRAM is demonstrated.

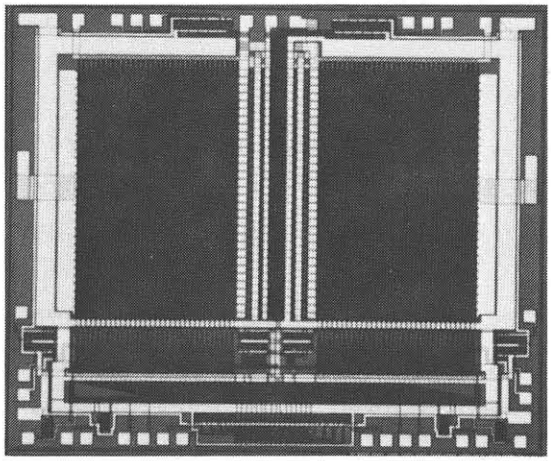

Fig. 1 Microphtograph of the 4kb SRAM chip.

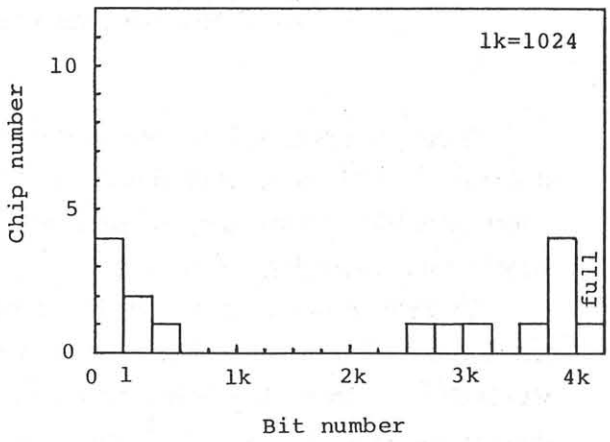

Fig. 2 Histogram for pass bit number.

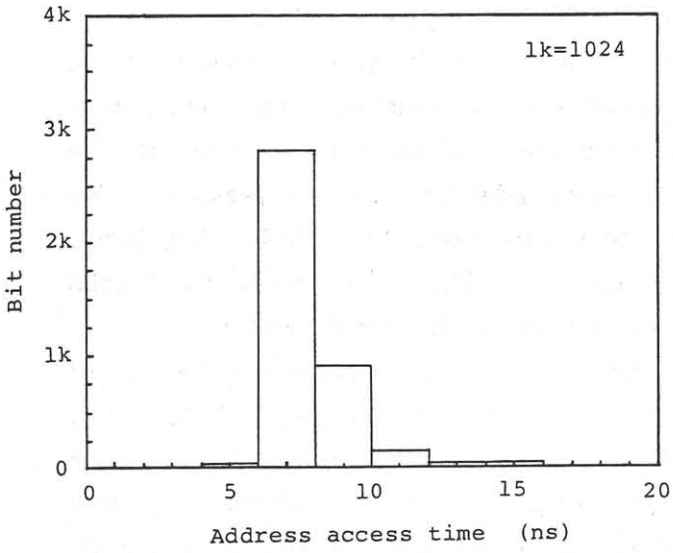

Fig. 3 Histogram for address access time.