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High Field Drift Velocity Measurement in Inversion Layers on Silicon

INVERSION LAYERS ON SILICON

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Over the past fifteen years, two important experimental techniques have been applied to the study of high field electron transport in silicon inversion layers. In this paper, we shall review the experimental work which has led to our present understanding.

I. Introduction

Modern MOS integrated circuits typically operate at a supply voltage of five volts, and employ transistors whose source-to-drain spacing is in the neighborhood of one micron or less. Under these conditions, the drain current of the transistor is limited by velocity saturation of the electrons in the inversion layer. In order to predict the electrical characteristics of these circuits, we need an accurate idea of the relationship between electron velocity and electric field in the inversion layer. The situation is complicated by the fact that the electron velocity depends on both the normal component of the field (i.e. the component perpendicular to the interface) and the tangential component (i.e. the component parallel to the interface).

At low tangential fields (less than 1 V/μm), the electron velocity is known to increase linearly with tangential field, and decrease in a more complicated manner with normal field. It is also known to be a strong function of processing, decreasing with fixed oxide charge Q_f and with surface roughness, but being essentially independent of doping. At tangential fields above about 1 V/μm, the electron velocity tends to saturate with increasing field, but the exact dependence of velocity upon normal and tangential field in this regime was not known until recently. In this paper, we shall review the work which has led to the present understanding of electron transport along the SiO_2-Si interface at high tangential fields.

II. The Conductance Technique

The first experimental measurement of the high field drift velocity of electrons in silicon inversion layers was reported in 1970 by F.F. Fang and A.B. Fowler [1]. They deduced the drift velocity from measurements of drain conductance as a function of drain-source voltage in n-channel MOS transistors of channel length 10 μm. Similar results were reported by T. Sato and co-workers in 1971 [2] for both holes and electrons. As shown in Fig. 1, the data of both groups indicated an electron saturation velocity in the neighborhood of 6×10^6 cm/s, a value well below the saturation velocity of 1×10^7 cm/s observed for electrons in bulk silicon [3]. In addition, the hole velocities extrapolate to a higher saturation velocity than electrons.

The measurement technique used by these workers was essentially an extension of the method used to determine the electron mobility at low fields. We shall

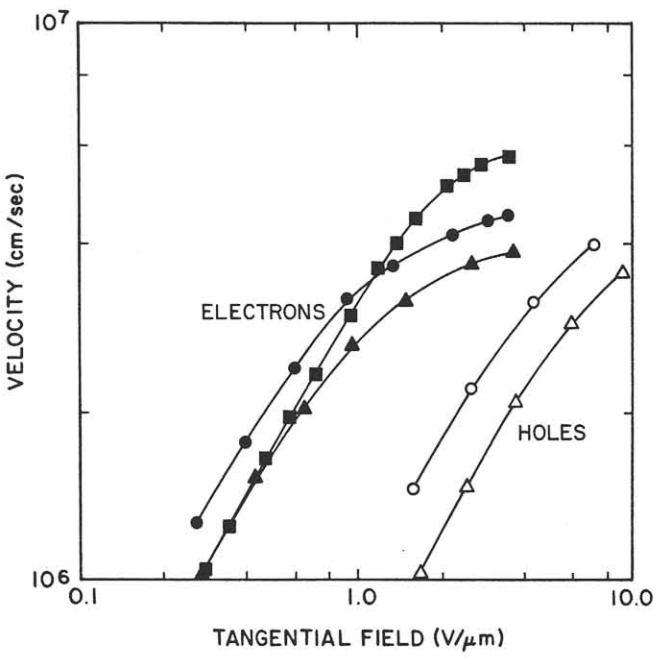

Figure 1. Electron velocity of Fang and Fowler (squares), and hole and electron velocity of Sato and co-workers on (100) MOSFETs at room temperature obtained by the conductance technique. The data of Sato, et al. were obtained at gate voltages of 30 V (upper curves) and 60 V (lower curves).

refer to this as the "conductance technique". At low tangential fields, the conductance technique is highly accurate, since the surface potential varies only negligibly from source to drain, and the electron density and field can be considered uniform along the channel. However, at high fields this assumption is not justified. Electron density, and both normal and tangential components of the electric field become strong functions of position, and the observed drain conductance then must be regarded as a weighted average of conditions along the channel. Under these conditions, it is no longer possible to attribute the measured conductance to a particular value of carrier velocity, or to a particular value of electric field.

In 1980, three groups reported the results of new work in this area. W. Muller and I. Eisele [4] modified the basic conductance technique, correcting for the variation in electric field along the channel by fitting to their data using an analytical model. They determined that the electron saturation velocity was approximately 8.5×10^6 cm/s, a value much closer to the bulk value.

R.W. Coen and R.S. Muller [5] reported measurements on a special resistive gate MOS transistor. By appropriately biasing the two gate contacts, they were able to create a uniform electric field along the channel, even at high tangential electric fields. They again determined the velocity from the ratio of the drain conductance (or drain current) to the electron density. Their data, shown in Fig. 2, exhibits low velocities for both electrons and holes.

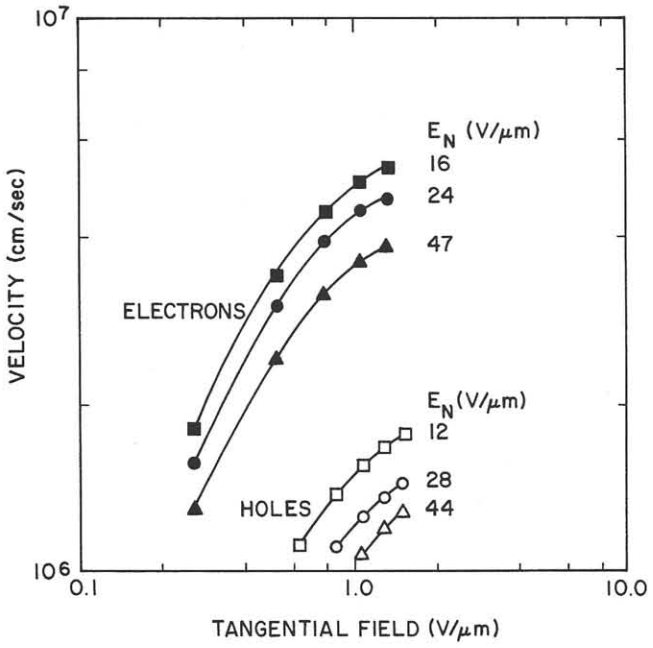

Figure 2. Electron and hole velocities obtained by Coen and Muller using a resistive-gate (100) MOSFET at room temperature. Effective normal field E_n is indicated.

The third measurement, reported by J.A. Cooper and D.F. Nelson [6], was the first to employ a technique in which the drift velocity was observed directly, rather than indirectly from the drain conductance. This technique has yielded the most detailed information on the high field transport properties of carriers at the SiO_2-Si interface, and we will review it in detail in the next section.

III. The Time of Flight Technique

In the time of flight technique [7], we observe the drift time of a packet of electrons introduced into the silicon surface region by a pulsed laser. As shown in Fig. 3, the experimental device is essentially an MOS gate-controlled diode with a long resistive gate. A voltage is established across the gate contacts in such a direction as to drive electrons toward the drain. The drain is biased positively with respect to the gate, so that any electrons in an inversion layer will be drawn off into the drain. The sample is then in a state of deep depletion, since any thermally generated electrons are quickly swept out.

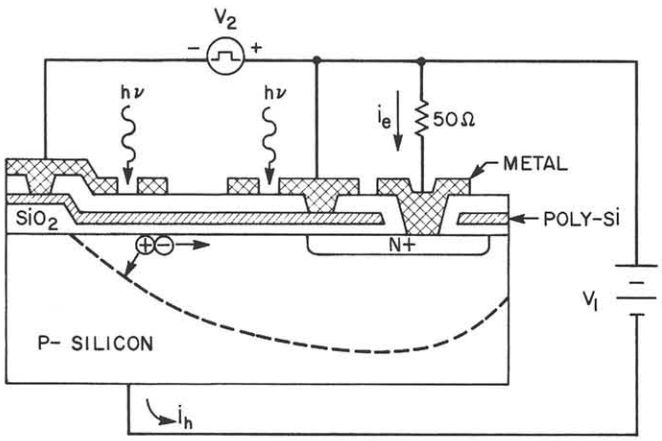

Figure 3. MOS resistive gate device used for the time of flight experiment. The polysilicon gate measures 100 μm between the interior edges of the contact windows, and the gate oxide is 0.1 μm thick.

Let us consider the situation when there are no electrons present in the inversion layer. If the silicon is lightly doped, say less than 5×10^{14} cm^{-3}, the surface depletion region will spread many microns into the semiconductor, and almost all of the gate voltage will be developed across the depletion layer, leaving only a small fraction developed across the gate oxide. Thus, the surface potential is nearly equal to the gate voltage at each point in the channel, at least in the absence of inversion electrons. Since the gate voltage increases linearly along the channel, the surface potential will also increase linearly with position. This results in a uniform tangential electric field along the surface in the

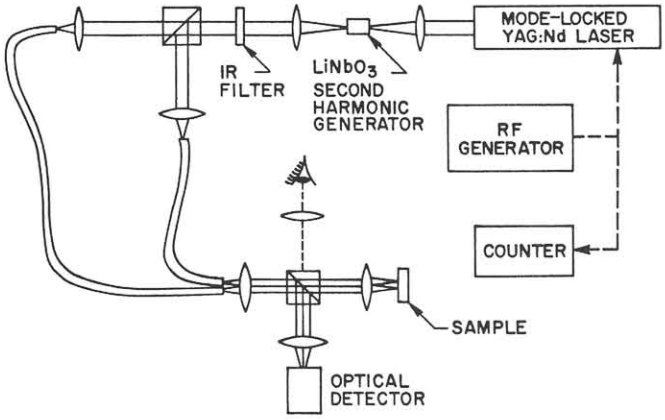

Figure 4. Experimental arrangement used to inject optical pulses into the two apertures of the time of flight device. The fibers are of different length to insure that two pulses are not present in the device at the same time.

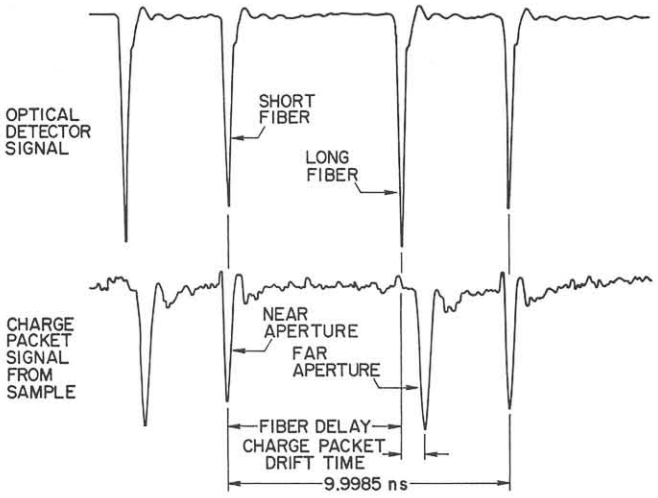

Figure 5. Waveforms from an optical detector viewing the core images of the fibers (top) and electrical pulses in the drain circuit of the device (bottom). The tangential field is 2 V/μm. The second and third optical pulses originated from the same laser pulse; the second traveled down the shorter fiber and the third traveled down the longer fiber. The short fiber is focused on the near aperture of the device and the long fiber on the far aperture. The lower waveform has been moved to the left so that the electrical pulse from the near aperture and it's optical pulse align. The additional delay in the arrival of the charge packet from the far aperture is obvious.

silicon. If we then introduce electrons at some point in the channel, say by photogeneration, these electrons will experience a uniform tangential field, and will drift along the channel and into the drain. As the electron packet enters the drain, a current pulse will be observed in the drain circuit. By measuring the difference in arrival times of packets introduced at different points in the channel, we can calculate the drift velocity.

The experimental apparatus is shown in Fig. 4. A mode-locked Nd:YAG laser produces a regular sequence of 100 ps pulses at 1.064 μm. These pulses are converted to 0.532 μm by a $LiNbO_3$ second harmonic generator. The beam is split and coupled into two multimode optical fibers of different length. The core images of the two fibers are focused on two optical apertures formed in the metallization level of the experimental device, with the short fiber focused on the aperture nearest the drain. Figure 5 shows the pulse waveforms from an optical detector and from the drain of the device. After accounting for the known time delay between the two fibers, it is apparent that the electrical pulse from the far aperture arrives after a delay relative to the pulse from the near aperture. This delay is due to the transit time of the electron packet across the separation between the apertures. Knowing the separation between apertures, we can calculate the drift velocity under the applied field conditions.

The tangential and normal components of the field in the channel can be controlled independently. The tangential field is determined by the potential V2, while the normal field is controlled by the substrate bias V1. Electron velocity is then measured as a function of tangential and normal field. Hole velocity is obtained in an analogous manner by using an n-type silicon substrate and inverting all the potentials.

Electron [7] and hole [8] velocities on (100) silicon at room temperature are shown in Fig. 6. We note immediately that for both types of carriers, velocities are significantly higher than those reported by earlier workers using the conductance technique, and that the electron saturation velocity agrees well with the values obtained by Muller and Eisele. The hole velocity does not saturate in the field range investigated by this technique.

While the low field velocity (and thus the mobility) of electrons decreases with normal field as expected, the electron saturation velocity is apparently not a function of normal field. Further, no significant variations were seen between samples fabricated on wafers having different substrate doping and fixed oxide charge.

Both hole and electron velocity-field curves can be fit by the empirical expressions

$$v = \mu E_t / [1 + (\mu E_t / v_s)^{\alpha}]^{1/\alpha} \quad (1)$$

$$\mu = \mu_0 / [1 + (E_n / E_c)^c] \quad (2)$$

where μ is the mobility, E_t and E_n the tangential and normal components of electric field at the surface, v_s the saturation velocity, μ_o the mobility at the limit of zero normal field, and E_c, α, and c are fitting parameters. The parameter values corresponding to the data in Fig. 6 are listed in Table I.

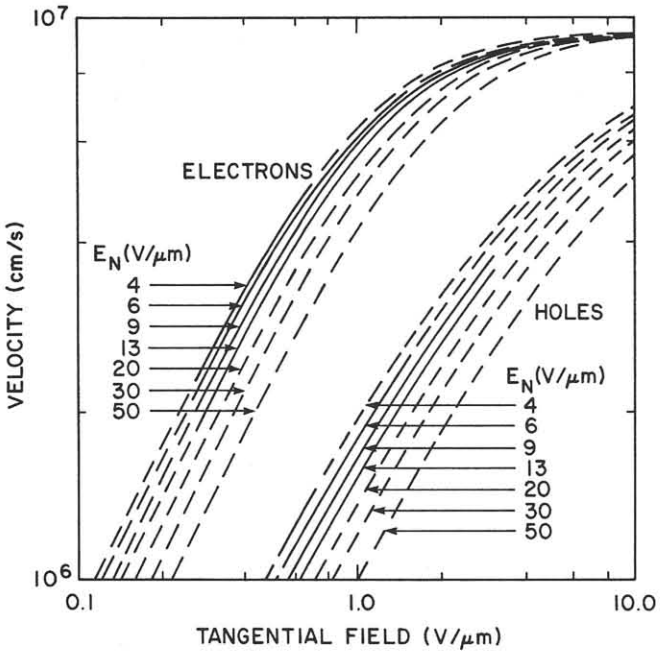

Figure 6. Electron and hole velocities obtained by the time of flight technique on (100) silicon at room temperature. Effective normal fields are indicated. The solid lines indicate the regions where data was taken; the dashed lines are extrapolations based on the empirical equations using the parameters in Table I.

Table I. Parameters for Electrons and Holes on (100) Silicon at Room Temperature.

Parameter	Electrons	Holes
$\mu_o(cm^2/Vsec)$	1105	342
$E_c(v/\mu m)$	30.5	15.4
c	0.657	0.617
$v_s(cm/sec)$	9.23×10^6	1×10^7
α	1.92	0.968

IV. Summary

Through the efforts of a number of workers over the past fifteen years, we now have a fairly accurate picture of the high field behavior of electrons and holes in inversion layers on silicon. The situation is complicated, both experimentally and theoretically, and much remains to be done. For example, we need more complete data on electron velocity as a function of temperature, and on hole velocity as a function of temperature and fixed oxide charge.

Considerable work has been done on modeling the high field transport processes in the inversion layer, both from a first-principles approach [9-11] and using semi-empirical models [12], but here too, the complexity of the physical situation presents problems. Part of the problem in arriving at the correct theoretical model stems from a lack of sufficient experimental data to fully determine the parameters of the models.

Considering the current trends in the VLSI industry, the economic importance of understanding the physics of electron transport at the SiO_2-Si interface has never been greater.

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