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An ECL Compatible 64Kb FIPOS/CMOS Static RAM

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Abstract

This paper describes newly proposed on-chip ECL interface circuits and cell array concept to realize a high speed and relatively low power dissipation CMOS SRAM. To verify these new technologies, a 64Kb, 8Kw x 8b, ECL compatible CMOS SRAM has been designed and fabricated, using advanced 1.5 μm FIPOS/CMOS process technology. An access time of 20 ns and power dissipation of 520 mW are observed.

1. Introduction

In recent years, the speed of MOS SRAMs has been improved drastically, and 64Kb chips TTL compatible with a sub 20 ns access time were reported.[1),2),3)] A sub 20 ns MOS SRAM can replace a bipolar ECL RAM. But in order to realize this, development of an ECL compatible I/O interface is indispensable.

As for an ECL compatible MOS SRAM, only the 4Kb chip was reported,[4)] using n-well bulk CMOS technology with bipolar devices. However, there are several problems with 4Kb chip, such as high power dissipation in its input buffer, insufficient ECL compatibility in its output buffer, etc.

In order to solve these problems, new input and output buffer circuits are proposed in this paper. Moreover, a new cell array concept is proposed to realize a low power SRAM. To verify these new technologies, a 64Kb ECL compatible CMOS SRAM has been designed and fabricated, using advanced 1.5 μm FIPOS technology[5)] which makes realization of an SOI structure on a silicon wafer possible.

This paper describes on-chip ECL interface circuits, a new cell array concept and experimental results.

2. On-chip ECL interface circuits

2.1 Input buffer

The newly developed input buffer consists of three stages, i.e., a level shifter, an inverting amplifier and an inverting buffer , as shown in Fig.1. The level shifter shifts input ECL levels downward. The shifted levels are controlled by the bias voltage, VB, sent from an on-chip control circuit, to assure that the inverting amplifier operates under high voltage gain conditions. The inverting amplifier amplifies the shifted ECL signal to an almost CMOS level. Therefore, the DC current of the amplifier is negligible. The inverting buffer provides full CMOS level swings to subsequent circuits.

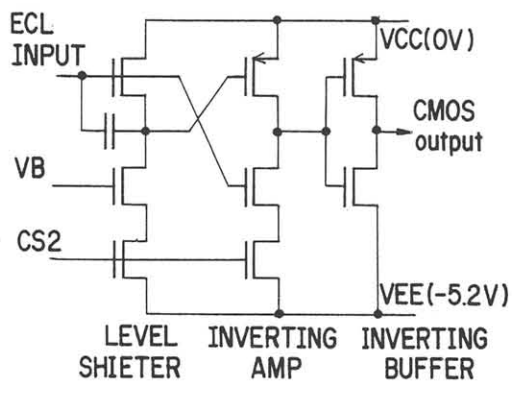

Fig.1 ECL to CMOS input converter

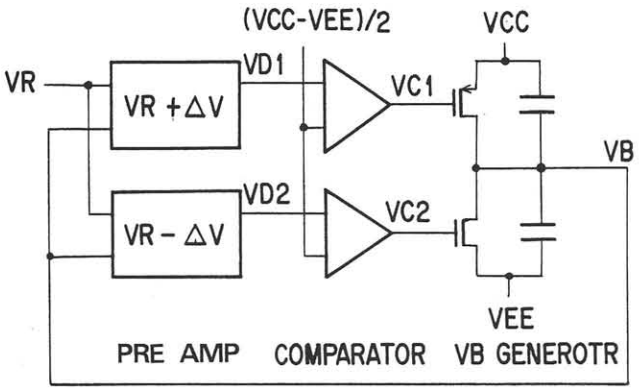

Fig.2 VB control circuit

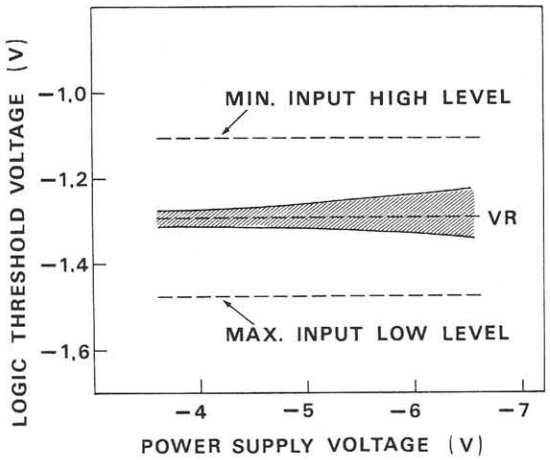

Fig.3 Logic threshold voltage versus supply voltage

Since the input buffer consists of a minimum number of stages and is designed to produce low DC current, high performance is achieved. The estimated values of the input buffer's power dissipation and delay time for ECL to CMOS level conversion are less than 10 mW and 3 ns, respectively.

In addition to high performance, the input buffer has sufficient operation margin and thereby allows variations in supply voltage, by controlling VB so as to make its logic threshold voltage VTL nearly equal to ECL reference voltage VR. VB is controlled by a VB control circuit which consists of two pre-amplifiers, two comparators and a VB generator, as shwon in Fig.2.

The pre-amplifier consists of the level shifter and the inverting amplifier shown in Fig.1. The two pre-amplifiers are designed to have logic threshold voltages of VTL1 (=VR+ΔV) and VTL2 (=VR-ΔV), respectively, and to be VTL1-VTL2 = 2ΔV (constant), even if supply voltage is changed. When VTL1 is lower than VR, both the output of the comparators, VC1 and VC2, are high and VB is lowered. On the other hand, when VTL2 is higher than VR, both VC1 and VC2 are low and VB is heightened. When VTL1 > VR > VTL2 is satisfied, VC1 and VC2 are VCC and VSS, respectively. Therefore, VB is not changed. In this VB control circuit, 2ΔV is designed to be 0.1V.

The VTL deviation dependence on the supply voltage is shown in Fig. 3. A VTL deviation less than ± 0.05V is achieved for the supply voltage variations of -4V to -6V, owing to the VB control circuit.

2.2 Output buffer

An output buffer circuit, converting an internal CMOS level signal to an ECL level signal and driving a 50 Ω external load, is shown in Fig.4. It consists of a CMOS inverter with a temperature compensated VSS generator, an open drain p-channel MOS transistor and two PN diodes.

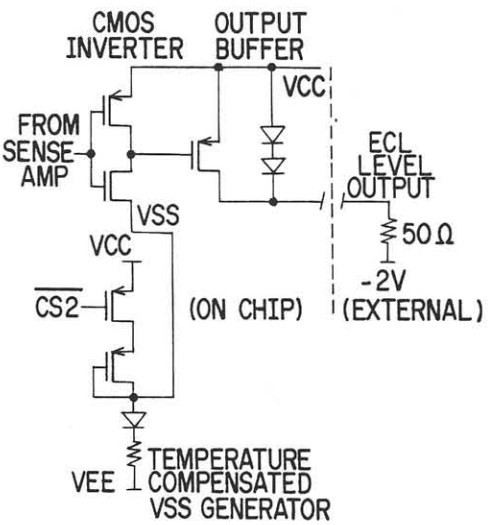

Fig.4 CMOS to ECL output converter

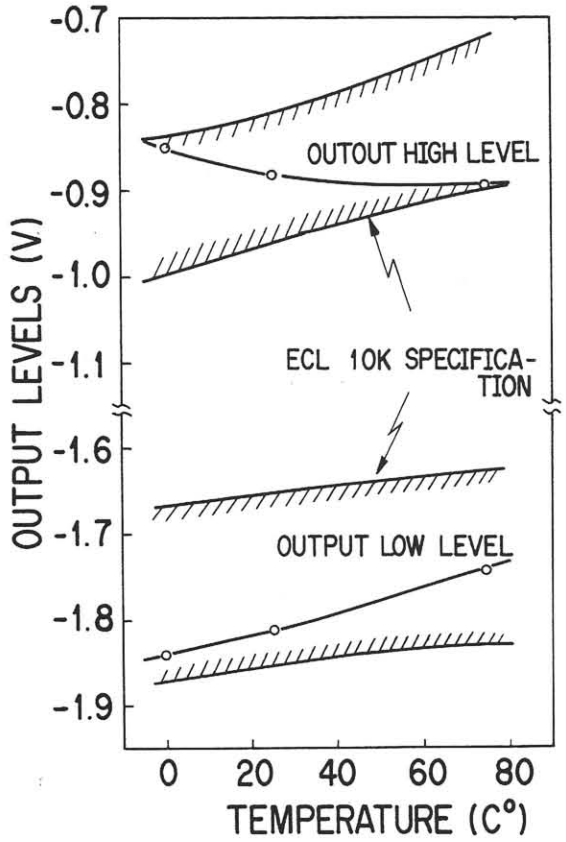

Fig.5 Temperature dependence of output levels

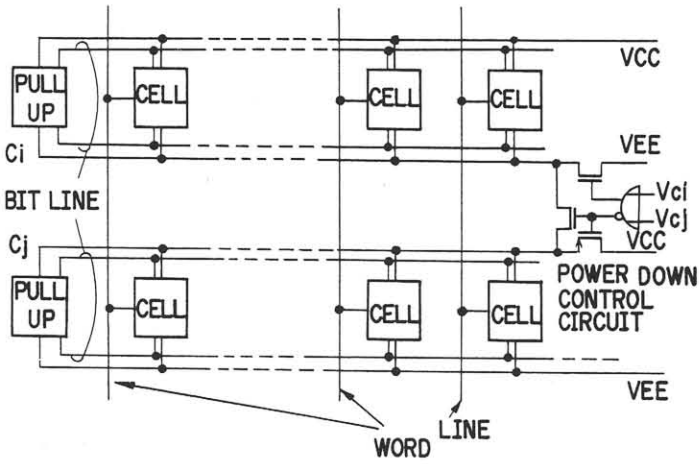

Fig.6 Cell array with power down control circuit

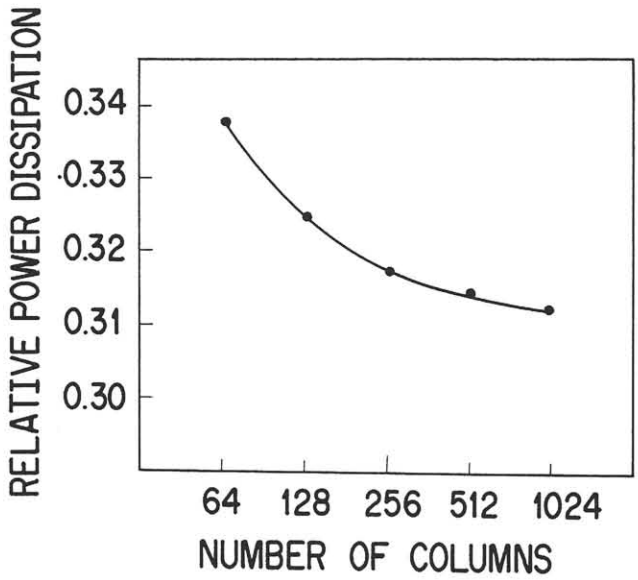

Fig.7 Relative power dissipation versus number of columns

The output high level is controlled by the CMOS inverter circuit and the p-channel MOS transistor. The low output is supplied by the two PN diodes connected in series.

The temperature dependence of the output high level is designed to be almost the same as the ECL 10K IC, owing to the temperature compensated VSS generator. The VSS generator consists of a MOS diode and a PN diode each with opposite threshold voltage temperature dependence. As the temperature increases, threshold voltage of both diodes shifts and lowers the VSS level. Therefore, the temperature compensated VSS generator can compensate for p MOS transistor output current decrease with increasing temperature. The measured temperature dependence of the output levels is shown in Fig.5. These results show that the output levels meet ECL 10K specifications.

3. New cell array concept

To achieve low power dissipation, a new cell array concept is introduced. The cell array is divided into many blocks, each of which consists of memory cells connected to a pair of columns, as shown in Fig.6. Figure 6 also shows a power down control circuit which controls the power supply path by using column select signals.

Full supply voltage (VCC-VEE) is provided to the memory cells in the two selected columns. On the other hand, only half of the supply voltage (VCC-VEE)/2 is provided to the remaining memory cells. Since only half the supply voltage is provided to most of the memory cells, the power dissipation of this cell array is reduced drastically.

The relative power dissipation as a function of the number of columns is shown in Fig.7. This cell array reduces the power dissipation to less than 1/3 that of a conventional cell array, for 128 or 256 columns corresponding to a 64Kb RAM.

4. Experimental results

A photomicrograph of the fabricated 64Kb SRAM, indicating the locations of major circuit blocks, is shown in Fig.8. Dimensions of the RAM chip are 6.0 mm x 8.64 mm. In order to reduce RC time delay of the word and bit lines, the SRAM is divided into four 16Kb arrays with each array containing 4Kw x 4b. The word organization of the SRAM is modified so as to be 8Kw x 8b.

An advanced 1.5 µm FIPOS/CMOS process technology was employed. Both effective channel lengths of the n and p MOS transistors are 1um. Operating waveforms of the fabricated SRAM are shown in Fig.9. The observed typical access time of this RAM is 20 ns. At the same time, a low power dissipation of 520 mW is attained. Its key characteristics are summarized in Table 1.

5. Conclusions

A 64Kb, 8Kw x 8b, ECL compatible CMOS static RAM was designed and fabricated, utilizing newly developed ECL interface circuits and a new cell array concept. Additionally, advanced 1.5 µm FIPOS/CMOS process technology was employed.

It was verified that the SRAM has a 20 ns access time and a power dissipation of 520 mW.

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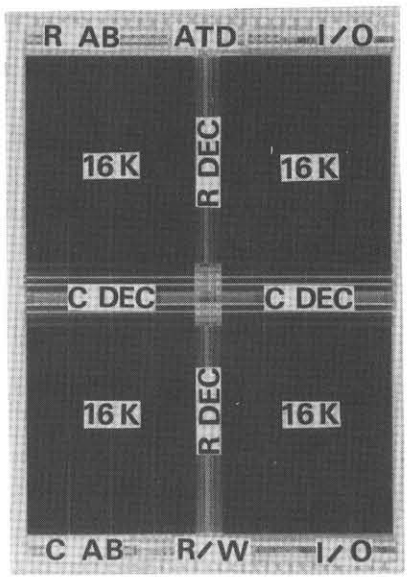

Fig.8 Photomicrograph of the 64Kb SRAM

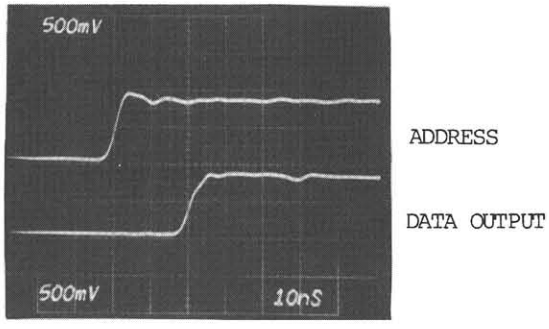

Fig.9 Operating waveforms of the 64Kb SRAM

Table 1 Summary of key characteristics and technology

Organization	8192 word x 8 bit
Cell size	20 µm x 25 µm
Chip size	6.0 mm x 8.64 mm
Access time	20 ns
Power dissipation	520 mW
Supply voltage	-5.2V
I/O interface	ECL compatible
Technology	1.5µm FIPOS/CMOS double-level Al 1 µm effective channel length