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Characterization and Performance Analysis of Masked LDD Transistor for CMOS VLSIs

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Masked LDD MOSFETs are proposed to improve the operation speed of CMOS VLSI circuits and to eliminate the process complexity of the side wall spacer technique. Characterization and performance analysis together with production feasibility study shows that the masked LDD structure has enough process margin, design flexibility, and superior performance than the side wall LDD structure except for the case that requires the dual directional current flow.

1. INTRODUCTION

The lightly doped drain (LDD) structure[1)2)3)] is considered to be most promising to obtain superior hot carrier resistance and higher substantial drain breakdown voltage. However, one of the serious limitation of the LDD MOSFET to the actual device application for VLSI comes from the reduction of conductance due to the increase of series resistance. Therefore the many efforts have been done to optimize the series resistance as well as keeping device reliability and performance[3)4)].

Introduction of the side wall spacer technique[4)5)6)] to the fabrication process for the LDD structure has been believed most suitable to control the length of n^- region and to minimize the series resistance. But at the same time, it increases the process complexity such as the RIE process of the CVD SiO_2 layer for the side wall spacer and it usually requires the special surface treatment to remove the contaminated and damaged layer. Moreover, the use of the side wall spacer introduces the undesirable n^- region to the source side. The purpose of this paper is to propose another approach to the idealized LDD structure which we called masked LDD structure[7)] improves the operation speed of CMOS VLSI circuits and eliminates the process complexity of the side wall spacer technique.

2. DEVICE STRUCTURE AND FABRICATION PROCEDURE

Figure 1 shows the masked LDD structure. The n^- region is determined by photo-lithography and placed only in the drain side to reduce the hot carrier degradation and obtain high breakdown voltage. The fabrication procedure based on the conventional polysilicon-gate FET process matched for 1.2 μm n-well CMOS process[6)]. After defining polysilicon gate, a blanket n^- ion (phosphorus) implantation is performed. After this step, the half of the drain side of the gate region and the drain n^- region are masked by photo-resist and is followed by n^+ arsenic-ion implantation step. This mask step is considered as a progressive mask step for n^+ ion implantation in the conventional CMOS process. Therefore, lightly doped n^- region is formed only between the gate edge and drain n^+ region without increasing the additional mask step or etching process.

The length of drain n^- region, Ln^-, are varied from 0 μm to 1.6 μm. The n^+ junction depth, X_j, is 0.22 μm. Gate oxide thickness is 28 nm.

3. RESULTS AND DISCUSSION

A. DEVICE CHARACTERISTICS

Figure 2 shows the I-V characteristics of three types of transistors with the conventional n^+ drain, the masked LDD, and the side wall LDD of n^- dose, $1 \times 10^{13} cm^{-2}$. Reduction of channel current in saturation region is not observed in the masked LDD MOSFET, therefore current drivability of the masked LDD MOSFET is essentially the same as that of conventional n^+ drain MOSFET. Figure 3 shows the typical variation of drain current, I_d, of the masked LDD MOSFET for the gate voltage V_g = 5 V, and the drain voltage, V_d = 5 V, as a function of drain n^- length, Ln^-. The stability of drain current in the saturation region with increasing Ln^- below 1.6 μm are confirmed and the dispersion is the same as that of conventional n^+ drain MOSFET. In this case the surface concentration of n^- region is $1.8 \times 10^{18} cm^{-3}$.

Figure 4 (a) shows the typical variation of

drain current in the linear region (V_g = 5V, V_d = 0.1 V). According to the increase of drain series resistance, the drain current, I_d, decreases with increasing the n^- length. Figure 4 (b) shows the Ln^- dependence of the channel resistance of the masked LDD MOSFET (V_g = 5 V). The increase of the channel resistance for the masked LDD MOSFET in linear region is given by

$$1/g = 1/g_o + R_s + R_d \quad (1)$$

$$\simeq 1/g_o + R_d \quad (2)$$

where g_o represent the intrinsic channel conductance, R_d is the drain resistance and R_s is the source resistance.

In the case of masked LDD MOSFET, source resistance, R_s, is negligible. There is a little difference at the Ln^- = 0 μm point for the masked LDD MOSFET and conventional n^+ drain MOSFET. The reason for this unconformity can be obliged to the difference of effective channel length between both type of MOSFET and to the local fluctuation of carrier path in lightly doped region under applied gate voltage.

Recent progress on photo-lithography enable us to keep the total error from the registration and from the pattern definition less than 0.3 μm. For example by setting the Ln^- 0.6 μm for the center value, the minimum Ln^- is expected as 0.9 μm and the maximum Ln^- as 0.9 μm. In this case the variation of drain current I_d in the saturation region is the same as that of the n^+ drain, and in the linear region 7 % is expected for the worst case. It will be shown later that the decrease of the channel conductance in the linear region is not serious problem for circuit operation through the CMOS ring oscillator analysis using SPICE simulator.

As the drain n^- length is shorter than that of the usual gate-contact spacing (for 1 μm to 1.2 μm devices, it is considered as 1.0 μm), the total area is not increase. This contribute to the reduction of junction capacitance of the masked LDD structure. It is true that the Ln^- will limit the gate-contact spacing for more scaled devices if there were no progress in pattern definition level.

B. PERFORMANCE ANALYSIS

Using previous device characteristics, delay time estimations for CMOS ring oscillator by SPICE were carried out.

Figure 5 shows the variation of delay time per stage, τ for 19 stage CMOS ring oscillator simulated as a function of drain n^- length, Ln^-. The gate length of n-ch MOSFETs and p-ch MOSFETs are 1.3 μm and 1.6 μm respectively. Channel width for both n and p-ch MOSFET are 10 μm. Total area of drain region for both n and p-ch MOSFET are 30 μm^2 (3 μm x 10 μm). As shown in Fig. 5, delay time are not changed by varing the Ln^- for the masked LDD MOSFET used for n-ch MOSFET and τ is the same as that of the n^+ drain MOSFET. On the contrary, the Ln^- dependence exists in the case of the side wall LDD MOSFET. The side wall LDD MOSFET with typical 0.3 μm Ln^- length causes about 3 % increase of delay time. In this simulation the junction capacitance and gate capacitance were assumed to be constant for the three types of MOSFETs.

In actual devices, by using LDD structure, the junction capacitance and the gate capacitance are expected to be reduced. In the case of the masked LDD structure, the junction capacitance decrease with increasing Ln^- and this will increase the switching speed. Figure 6 shows the estimated reduction rate of the total capacitance for n-ch MOSFET, where the device feature size is the same as that of used in the previous ring oscillator. Here the junction capacitance of n^- region was assumed as the 40 % of the n^+ region. It is estimated that the total capacitance of the masked LDD MOSFET with Ln^- = 1.0 μm is reduced by about 12.5 % compared with the n^+ drain MOSFET.

The characteristics also indicates the limitation of the masked LDD MOSFET. It decrease the circuit performance when it applied to the device which requires the dual directional current flow and also requires the n^- region both sides of the gate electrode, such as the transmission gate.

C. RELIABILITY

Hot carrier resistance versus various process parameters especially for n^- length, Ln^-, are examined. Figure 7 (a) shows the I_d degradation rate $\Delta I_d/I_d$ as a function of the stress time . The hot carrier stress conditions were chosen for the maximum substrate current, I_{sub} . Figure 7 (b) shows the I_d degradation rate after 10^4sec as a function of I_{sub}. Figure 7 (a) and 7 (b) clearly show the longer Ln^- gives longer device life time, which is due to the reduction of substrate current by longer Ln^-. As shown in Fig. 7 (b), I_d degradation rate shifts along the characteristic line with increasing the n^- length, Ln^-. For example, n-ch MOSFET with Ln^- = 1.6 μm has twice as long life time as that with Ln^- =0.4 μm. These results strongly suggest that the degraded area is strictly limited near the gate edge in n^- region which predominantly determines the device reliability.

The substrate current sensitivity for device degradation rate depends upon the surface concentration of the n^- region and the channel profile especially to the boron concentration of the deep channel region, N_{AP}. The higher n^- concentration, the lower N_{AP} and the longer Ln^- reduce the device degradation rate.

4. CONCLUSION

Characterization and performance analysis together with the production feasibility study shows that the masked LDD structure has enough process margin, design flexibility for hot carrier stress, and superior performance than the side wall LDD structure. Masked LDD MOSFET having high transconductance due to the absence of the the increase of series resistance, will be a promising structure for high density CMOS devices.

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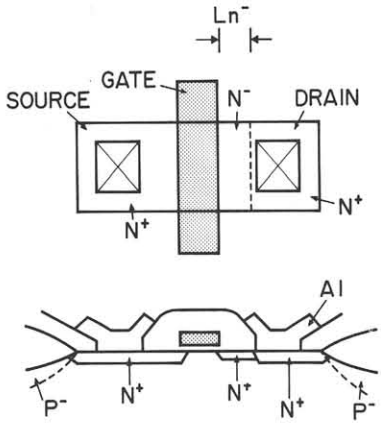

Fig. 1 Masked LDD structure.

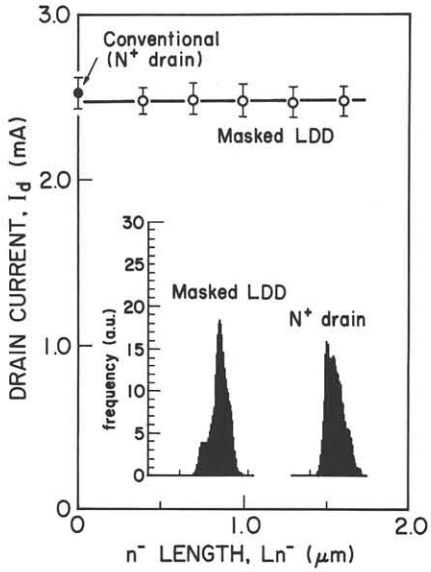

Fig. 3
Drain current, I_d, of the masked LDD MOSFET as a function of Ln^- (V_g=5V, V_d=5V). Typical dispersion of I_d is also shown compared with the n^+ drain MOSFET.

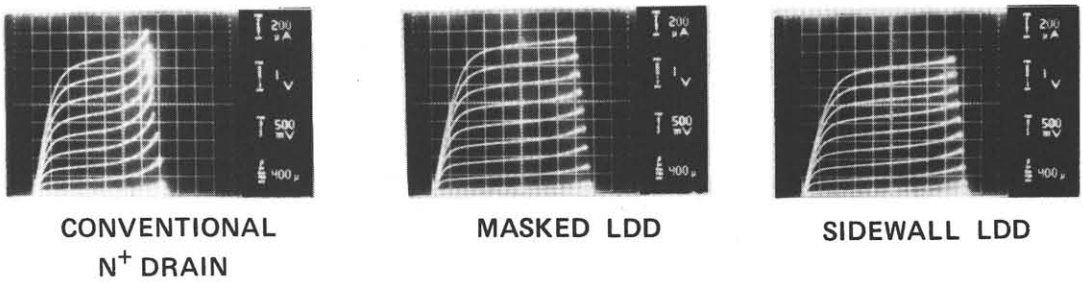

Fig. 2
I_d-V_d characteristics of three Types of MOSFETs with n^+ drain, the masked LDD, and the side wall LDD. W/L = 5 um/1.2um, Vth = 0.8 V.

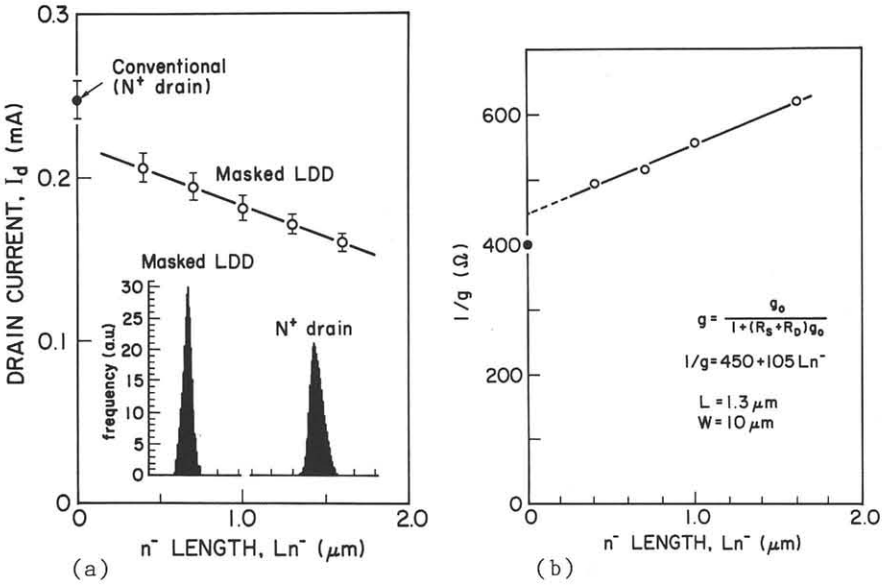

Fig. 4
(a) Drain current, I_d, and (b) channel resistance of the masked LDD MOSFET as a function of the drain n^- length. Typical dispersion of I_d are also shown compared with the n^+ drain.

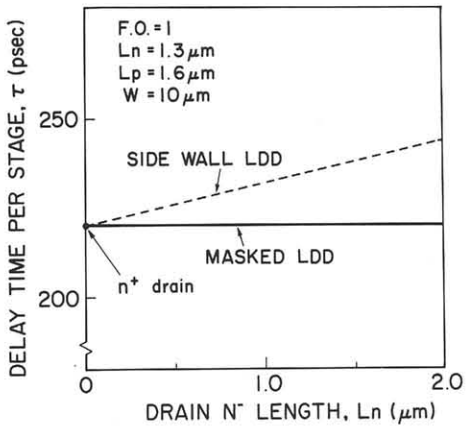

Fig. 5
Variation of delay time per stage for 19 stage CMOS ring oscillator simulated by SPICE as a function of the drain n^- length.

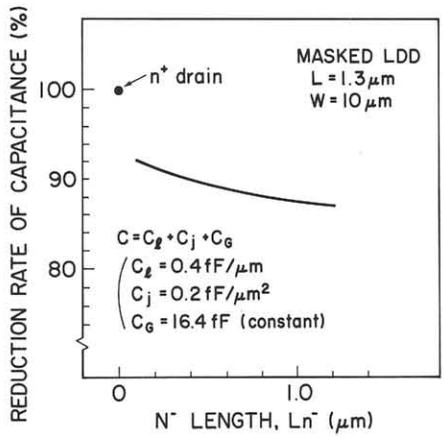

Fig. 6
Estimated reduction rate of the total capacitance of the masked LDD MOSFET as a function of the drain n^- length. The total area of the drain region is assumed to be constant.

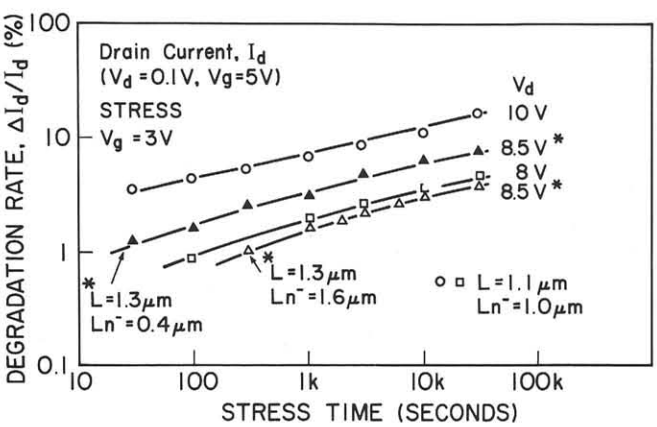

Fig. 7(a)
I_d degradation rate $\Delta I_d / I_d$ of the masked LDD MOSFET as a function of the stress time.

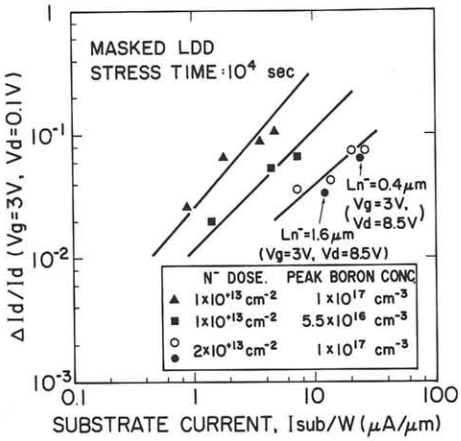

Fig. 7(b)
I_d degradation rate of the masked LDD MOSFET after 10^4 second stress as a function of the substrate current.