Extended Abstracts of the 17th Conference on Solid State Devices and Materials, Tokyo, 1985, pp. 29-32

A New Self-Aligned Contact Technology for LDD MOS Transistors

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A new self-aligned contact technology, which has a superior process compatibility with the LDD transistor fabrication, is proposed. This technology does not require the oxidation of the gate material. The Si_3N_4 film which covers gate electrodes is utilized as a interlevel insulator between gates and interconnections and also as spacers for LDD structure.

The process sequence and the results of Si_3N_4 insulator breakdown voltage, the transistor characteristics and the reliability are described.

1. Introduction

For high packing density MOS LSIs, the reduction of registration tolerance as well as fine pattern formation is required. Especially, the registration tolerance is now emerging as a major factor limiting further size reduction of source/drain regions. Therefore, the self-aligned contact technology which requires no registration tolerance has been proposed, in which the thermal oxide of gate polysilicon has been used as an interlevel insulator between gates and interconnections (1-4).

On the other hand, as the size of MOS transistor has been reduced, Lightly Doped Drain (LDD) structure has become necessary for minimizing hot carrier effects (5,6), and it is favorable to use refractory metals as gate materials to reduce signal delay. Moreover, as for the fabrication process, gate patten size must be well-controlled, and low temperature process is promissing.

In this work, we propose a new self-aligned contact technology, which has a superior compatibility with LDD MOS transistor process, and make it possible to utilize gate materials like refractory metals, because it does not need the oxidation of gate surface. In this technology, gate electrodes are covered with Si_3N_4 films by the use of the anisotropic etching of Si_3N_4 to form side-walls, and selective etching of SiO_2 to Si_3N_4 for opening contact holes to source/drain regions.

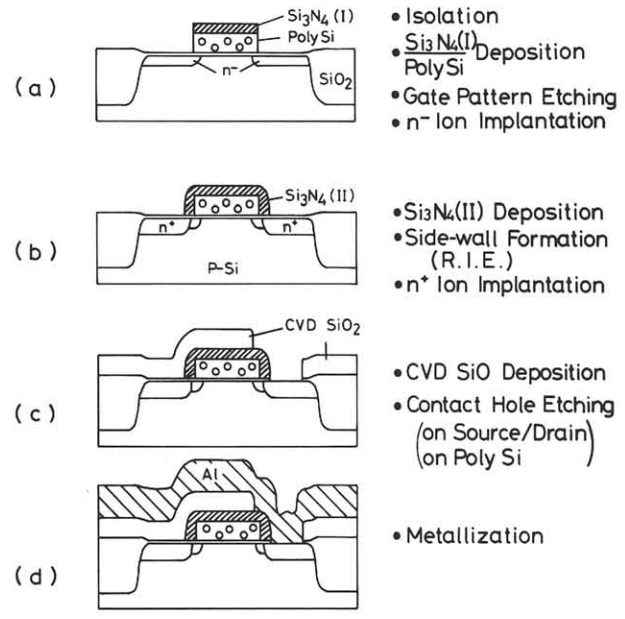

Fig.1. Process sequence of the new self-aligned contact technology.

2. Process Sequence

The process sequence of the new self-aligned contact technology which is adopted to n-MOS process is shown in Fig.1.

(a) Gate Delineation

Silicon substrate is P-type (100) of about 10 Ω·cm. After the formation of field isolation,

20 nm thick gate oxide is thermally grown. An n^+-polysilicon film of about 300 nm and LPCVD Si_3N_4(I) film are deposited successively. Si_3N_4 (I)/n^+-polysilicon bilayer is patterned into gate electrodes, and then n^--diffusion regions for LDD transistor are formed by phosphorus ion implantation with a dose of 7×10^{12} cm^{-2} at 40 keV.

(b) Side-wall Formation

Si_3N_4(II) film is deposited by LPCVD, and the film is etched by anisotropic reactive ion etching using CH_2F_2 gas as an etchant. Thus, the side-walls are formed on both sides of the polysilicon gate. Spacer width is almost the same as the thickness of the deposited Si_3N_4(II). Then arsenic ion implantation is carried out at a dose of 4×10^{15} cm^{-2} at 80 keV for the source/drain regions.

(c) Contact Formation

CVD SiO_2 film is deposited as a second interlevel insulator, on which the contact hole pattern is delineated by photoresist. The contact holes on the source/drain regions are patterned so as to touch or cross the gate electrode edges. The CVD SiO_2 film is etched selectively by using a combination of dry and wet etching. Thus the self-aligned contacts on source/drain are formed. Since the CVD SiO_2/Si_3N_4 bilayer is deposited on the gate electrodes, additional contact hole etching is necessary.

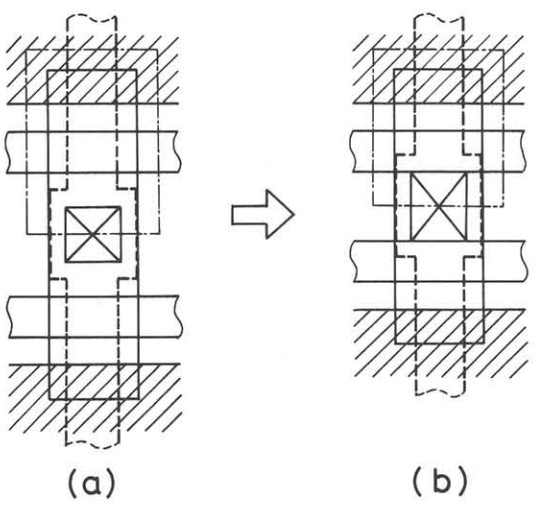

Fig.2. An application example of the self-aligned contact technology for dynamic RAM cell.
(a) layout pattern with conventional contact.
(b) layout pattern with self-aligned contact.

(d) Metallization

Finally, the device is completed after metallization.

The breakdown voltage of Si_3N_4 insulator is measured using the comb-like gate pattern which is fabricated on the thick SiO_2 film and covered all over with aluminum.

3. Application

This self-aligned contact technology is useful for high packing density MOS LSIs, especially MOS memories such as RAMs and ROMs.

Fig. 2 shows the layout patterns of dynamic RAM cells using (a) conventional contact technology and (b) this self-aligned contact technology. In this example, trench capacitor type d-RAMs based on around 1 μm-rule are assumed. The cell size reduction of about 15 % is obtained. Though the parasitic capacitance between the gate and the bit line interconnection increases by using the self-aligned contact technology, the bit line capacitance is nearly equal to that using the conventional contact, because the junction capacitance decreases by the area reduction of diffused region between the gates.

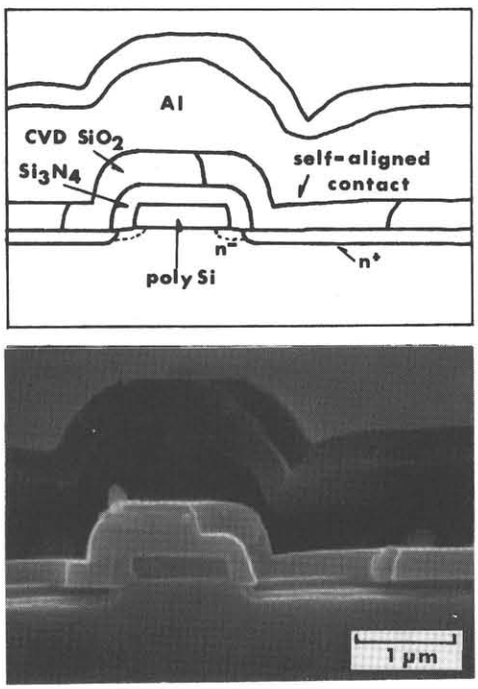

Fig.3. Cross-sectional view of self-aligned contact.

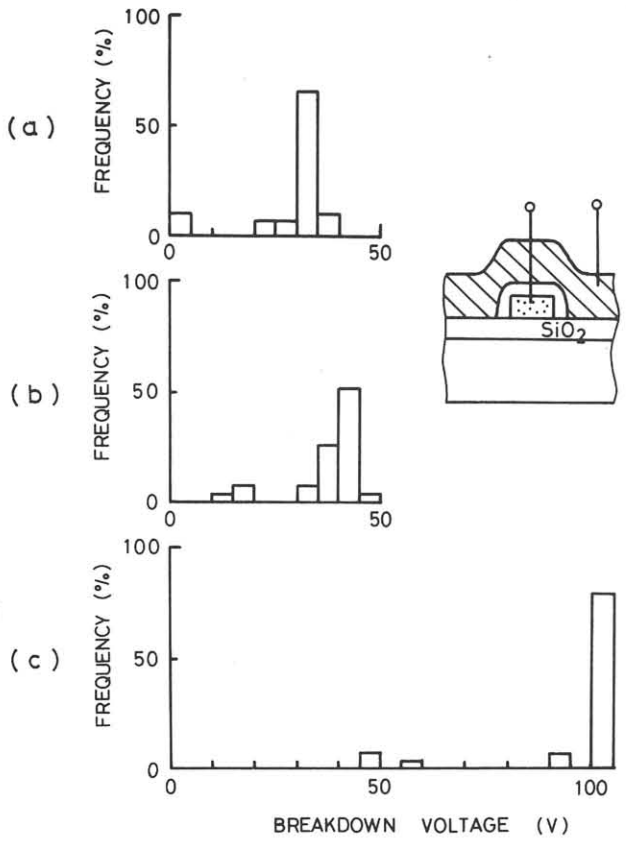

Fig.4. Breakdown voltage distributions of Si_3N_4 insulator.
Si_3N_4(I)/Si_3N_4(II) (a) 100nm/100nm, (b) 100nm/200nm, (c) 200nm/200nm

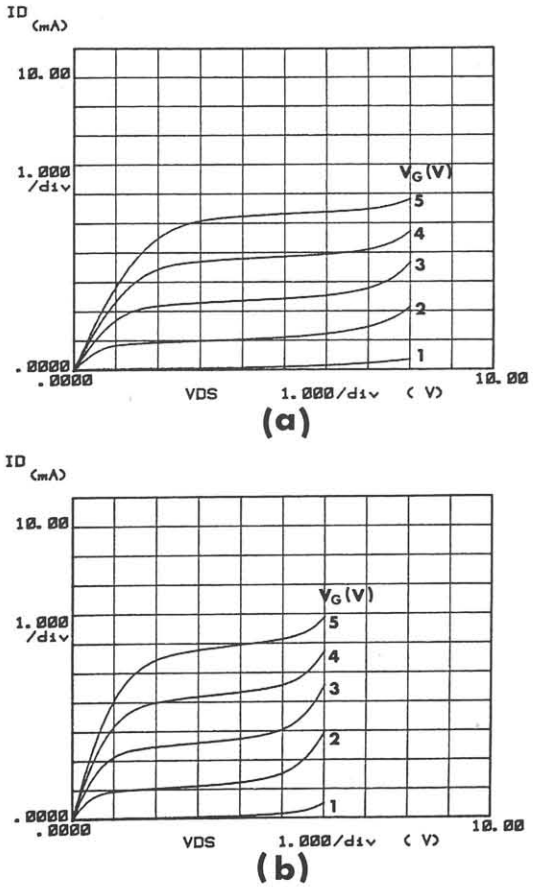

Fig.5. I_D-V_{DS} characteristics.
(a) LDD MOS transistor fabricated by the new self-aligned contact process.
(b) Conventional transistor.
(L=1.2 μm, W=20 μm)

4. Results and Discussion

1) Contact shape

Fig. 3 shows a SEM micrograph of the cross-section of the self-aligned contact using this new technology. This is an example when the thickness of Si_3N_4(I) and Si_3N_4(II) are both 200 nm, and the extent of the overlap between the gate electrode and the contact is rather large to show the good step coverage of Si_3N_4, though less overlap is favorable practically.

When the contact hole etching is carried out only by dry etching, the SiO_2 side-walls are attached on the Si_3N_4 side-walls, reducing the contact area.

2) Breakdown Voltage of Si_3N_4 Insulator

The histograms of breakdown voltages of Si_3N_4 insulator between n^+-polysilicon gate and aluminum electrode are shown in Fig. 4. In this figure, the breakdown voltages of more than 100 V are shown together by > 100 V, because of the applied voltage limit of the measuring apparatus.

Fig. 4 shows the dependence of breakdown voltage on Si_3N_4 thickness, in which the thickness of Si_3N_4(I) and Si_3N_4(II) range from 100 to 200 nm. The breakdown voltage seems to be determined by the Si_3N_4 thickness at the shoulders of the gate edges. Since there is little variation of the distributions of the breakdown voltages when n^+ ion implantation is omitted, n^+ ion implantation may not affect the breakdown voltages of the Si_3N_4 insulator obviously. When either Si_3N_4(I) or Si_3N_4(II) is 100 nm in thickness, there are some samples with low breakdown voltages which may be caused by the instability of the thin side-wall formation. When both Si_3N_4(I) and Si_3N_4(II) are 200 nm, minimum and typical breakdown voltages are 45 V and > 100 V, respectively. Although the distribution is a little scattered, these breakdown voltages are sufficiently higher than 20 nm gate oxide dielectric breakdown of about 25 V.

Therefore, this Si_3N_4 insulator can be used as interlevel insulator of MOS transistors.

3) Transistor Characteristics and Reliability

Fig. 5 shows I_D-V_{DS} characteristics of (a) LDD MOS transistor fabricated by this self-aligned contact process and (b) conventional MOS transistor. Both are L=1.2 μm, W=20 μm, and Si_3N_4 spacer width of LDD transistor is 0.2 μm. The improvement of the characteristics by the Si_3N_4 side-walls is almost the same as that by the SiO_2 side-walls. The characteristics do not depend on the degree of the overlap between the gate electrode and the contact.

In LDD transistors, the degradation induced by hot carrier effect has become a serious problem in the reliability (7). Fig. 6 shows transconductance (Gm) degradation of the LDD transistor fabricated by this technology which has the same size as shown in Fig. 5. The stress condition is V_G=3 V and V_D=8 V and Gm is measured at linear region. There is some degradation in Gm which is also observed in the LDD transistor with the SiO_2 side-walls. At the same time, V_t shift is measured under the same stress. The V_t shift is less than 5 mV at 2×10^4 sec. Since there is not much difference in the degree of the degradation between the Si_3N_4 side-walls and the SiO_2 side-walls, the optimization of LDD structure with the Si_3N_4 side-walls would be possible by the same way as that with the SiO_2 side-walls.

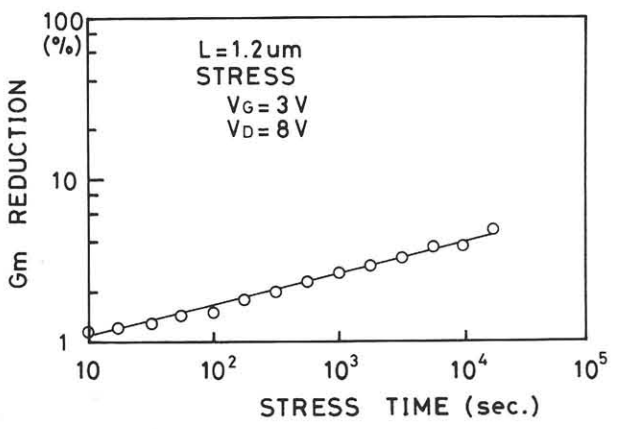

Fig.6. Time dependence of Gm degradation.

5. Conclusion

A new self-aligned contact technology with Si_3N_4 covered gate electrodes is proposed. This technology has a good process compatibility with LDD MOS transistors. Since this technology needs no high temperature oxidation process, the applications for submicron transistor fabrication which required low temperature treatment and for refractory metal gate transistors are possible.

As an interlevel insulator, Si_3N_4 film which covers the gate electrodes has sufficiently high breakdown voltage. The characteristics of LDD transistor with the Si_3N_4 side-walls and the reliability for hot electron effect are almost the same as those of LDD transistor with the SiO_2 side-walls.

Acknowledgement

The authors wish to thank Dr. H. Mizuno, Dr. S. Horiuchi and H. Esaki for their encouragement and advice. We would also like to express our gratitude to Y. Nakata for the reliability test.

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