Extended Abstracts of the 17th Conference on Solid State Devices and Materials, Tokyo, 1985, pp. 33-36

Comparison of α-Particle Induced Charge Collection on MOS Capacitors Using a DC Tester

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Results of α-particle induced charge collection measurements are presented for both depletion (ion implanted surface) and intrinsic (NO ion implanted surface) type capacitors. A new measurement method using a DC tester was applied to obtain the data. Also, a comparison is made between the amount of charge which has been collected using α-particles with different energy. The data confirms claims made that the charge collected is directly related to depletion layer depth.

INTRODUCTION

May and Woods [1] first described the problem of "soft errors" occurring in dynamic RAMs in 1978. Based on this initial observation, much work has been done to try to better understand this phenomenon. The soft error rate (SER) for DRAMs has been modeled and numerically calculated as functions of energy [2,3], and of DRAM cell type [4]. However, it is important to understand the funneling effect to determine the SER. A numerical study by Hsieh, et. al. [5] introduces the fundamental mechanism behind funneling. An analytical study was also reported [6], as well as measurements of charge collected on test structures [5,7,8]. The idea of reflecting barriers was also presented as an aid to reduction of charge collection [7,9].

Of the experimental work accomplished up to this point, SER has been measured [7] by placing various intensity α-sources in the vicinity of DRAMs and extrapolating SER for expected α-particle flux rates. In addition, charge collection measurements have been done on reverse-biased diodes [7,8] and MOS capacitors [8,10]. The techniques presented previously have all been AC, either by use of oscilloscope systems, or charge sensitive preamp and multichannel analyzer systems.

The purpose of this paper is to present a method for charge collection using a DC tester on MOS capacitors. This method will also be applicable to reverse-biased diodes whose surface potential is floating. This is an important consideration since the SER is dependent on both memory cell errors (soft errors which occur when an α-particle strikes a capacitor), and bit line errors (soft errors occurring when an α-particle strikes a bit line). Errors can also occur when an α-particle strikes peripheral circuits, but these circuits take up less chip area than the cell array. The most significant point of this method is the realization of charge collection on floating nodes, making the results more directly applicable to DRAMs.

MEASUREMENT METHOD

Consider a DRAM memory cell. The basic structure is composed of a bit line, a word line, and a storage capacitor. Data from a bit line (in terms of voltage) is transferred to the storage capacitor via the word line transistor. For a p-type substrate, a "1" is stored when the capacitor is in the deep depletion state. Similarly, a "0" is stored when the capacitor's surface is inverted. When an alpha particle strikes the capacitor, electron-hole pairs are generated in the substrate which can be collected by the capacitor in the "1" state by funneling and diffusion [5], while a "0" state capacitor will remain unchanged. Thus, a soft error will occur.

The devices used in this measurement were specially designed test structures which are very similar to dynamic memory storage cells. Figure 1 is the equivalent circuit of the test structures. In the figure, the substrate bias is labelled Vb. The voltage Vin corresponds to the bit line voltage, while Vtransfer corresponds to the word line voltage. Vcap is the storage capacitor plate voltage. In addition to the storage capacitor structure, there is an additional shallow implant directly adjacent to the capacitor surface. This implant is connected to the gate of a monitor transistor.

The source of the monitor transistor, Vs, is

held at ground potential and a small voltage is applied to the drain, Vd. With the bulk potential at -3 volts, and the capacitor plate voltage held at +5 volts, the transfer gate voltage is turned on to +8 volts and the input voltage, Vin, is ramped from 0 to +5 volts. The input voltage is directly connected to the gate of the monitor transistor. The drain current is measured in order to obtain an I-V calibration curve.

A charge decay curve can be obtained by holding the same bias conditions on the monitor transistor drain and source, and on the bulk and capacitor plate. The input voltage, however, is fixed at +5 volts while the transfer gate is turned on momentarily in order to deplete the capacitor surface. When the transfer gate voltage decreases to 0 volts, charge which is generated thermally begins to flow into the capacitor which is in deep depletion.

Figure 2(A) is a typical charge decay curve which is obtained by this method. A DC tester is used (HP4145) which samples data at specific intervals of time. As is seen, the time for charge decay can be very long.

Figure 2(B) is for the same measurement conditions, except that an α-source has been placed on the chip (as a lid). When an α-particle strikes the capacitor, charge is collected very quickly both by funneling and diffusion. This is what is believed to have happened for the large voltage jump. The charge generated by alpha particles which do not directly strike the capacitor can be collected by diffusion. This is the reason for the increase in slope of charge decay curve B.

Knowing the capacitance of the collection region, the amount of charge per voltage shift can be calculated. This can be done for each measurement interval (in this case, each 0.25 sec.). A histogram of this data is shown in figure 3. This shows the total number of data for each amount of charge collected.

Since the α-source flux is known as well as the collection area, the total number of alpha particles striking the capacitor can be calculated. When this is compared to the histogram data, it is seen that the total number in the cross-hatched region is equal to that calculated (within expected error). Thus, we conclude that the right hand side of the data correspond to direct α-particle strikes. An average value can then be calculated.

In addition, however, there is a "background" diffusion charge due to α-particles which do not directly strike the capacitor. This is the large amount of data on the left hand side of the histogram. Thus, the average "background" diffusion charge can be calculated and subtracted from the previous value to yield only the charge deposited due to one alpha particle.

MODEL FOR CHARGE COLLECTION

When an α-particle strikes a silicon wafer, e-h pairs are generated along the column of the track. Approximately 3.6 eV is required to generate 1 e-h pair. For an alpha particle with energy from 2 to 8 MeV, the range in silicon is from 10 to 60 microns. In addition, the charge is generated in straight line path along the direction of the α-particle. The carriers are generated within a radius of approximately 0.1 microns [8].

Even though the range and total number of e-h pairs created is determined by the initial energy of the alpha particle, the charge density is a function of the alpha particle speed. The density is seen to increase as the α-particle slows down, then dropping to zero very rapidly at the end of the track.

On the average, this yields an e-h pair density of $\sim 10^{18}$ cm^{-3} along the α-particle column. This is a very high concentration. Immediately after generation, ambipolar diffusion takes place and the charge spreads out radially. If a depletion region is struck, the electrons in the column move to the more positive potential and the holes move away from it. For a p-type substrate, the electrons are pulled in from farther along the track and holes are pushed out of the depletion region. Since the column carrier concentration is so high compared with the background, the potential distribution is modified to the extent that an electric field appears along the column of generated carriers so that a "funneling effect" occurs. In addition, diffusion of carriers not collected by funneling takes place.

This process is very complicated since the electric fields generated in the column depend upon the concentration of carriers. This concentration , however, varies as a function of time due to the electric field moving the charge. A general description requires the solution of Poisson's equation along with the hole and electron continuity equations. Computer solutions were done by Hsieh et. al. [5].

A simple equation was developed by Hu [6] which describes the length along the column track to which the electric field can collect charge. We will use this same equation.

$$Lf = (1+\mu_n/\mu_p)*W/\cos(\theta)$$

Where Lf = funnel length
μ_n, μ_p = electron, hole mobility
W = depletion layer width
θ = α-particle incidence angle

The total length of the alpha particle track is known from the initial energy. We assume that the passivation glass layer of ∿1μ has the same stopping power as the silicon. Therefore, this distance is subtracted from the total alpha track length. The charge deposited as a function of distance is known, so using the equation above, the total charge in a length of column length Lf can be calculated.

RESULTS

The test structures are found on two different p-type wafers of 10 Ω-cm resistivity. On one wafer are capacitors with an area of $42\mu^2$ and the other with capacitors of $64\mu^2$ area. On the wafer with the $42\mu^2$ capacitors, two different types were built. One will be called depletion type, since it has an Arsenic implant under the gate. The surface concentration of the implant is $\sim 2*10^{17}$ cm^{-3} and has a junction depth of ∿0.1μ. The other will be called intrinsic, since it does not have any implants under the capacitor gate. Likewise, the $64\mu^2$ capacitor is intrinsic. The gate oxide thickness is ∿430A of SiO_2.

As a function of surface potential, the depletion layer width can be calculated. The average value is found to be ∿2.6μ for the depletion type capacitor. The intrinsic capacitor's average depletion layer width is ∿2.3μ.

Using the equation introduced previously, the funneling length is calculated for normal incidence alpha particles. Since the concentration of generated carriers in the column is very high ($10^{18}cm^{-3}$), compared to the substrate ($10^{16}cm^{-3}$), we can not necessarily use the same mobility values as that for low level injection of carriers into the bulk. Carrier-carrier scattering also plays a role which reduces the mobility of both the electrons and holes. Also, the mobility changes very rapidly as a function of time since the electrons are being collected very fast. Thus, we use mobility values of 200 and 110 cm^2/V-sec for μ_n and μ_p respectively. Funneling lengths of 7.3μ and 6.4μ are calculated for depletion widths of 2.6μ and 2.3μ.

Two alpha sources with energies of 4.4MeV and 3.3MeV were used in the measurements. This corresponds to a total penetration depth of ∿19μ and ∿13μ respectively in the silicon. From the knowledge of the amount of charge deposited as a function of distance, the charge in a length of 6.4μ and 7.3μ was calculated. This is shown in Figure 4. Also in this Figure is plotted the measured data. Table 1 shows the data in numerical form. The data plotted and shown in the table are averaged over ten devices measured. Assuming that the charge collected by drift is contained in the funneling length, the percentage of drift collected charge is calculated and presented. The remainder is due to diffusion and is also shown.

CONCLUSIONS

We can see in Table 1 that the amount of charge collected for the lower energy alpha particle is greater than that for the higher energy one. When the data is plotted as in Figure 4, we see that it seems to follow the same type of curve as that which has been calculated due to funneling. This gives us evidence to the fact that the charge collected depends very strongly on the funneling effect.

Another conclusion that we can draw from the data is the dependence of charge collection on depletion layer width. We see that the depletion type device collected more charge than the intrinsic type device. We also see that it occurs in approximately the same ratio. That is, the ratio of depletion layer widths is 2.6μ/2.3μ ≈1.1. The ratio of charge collected for the 3.3 MeV alpha particle is 99fC/90fC ≈1.1. For the 4.4 MeV alpha particle, 86fC/70fC ≈1.2. Both charge collection ratios are close to the depletion width ratio. This points to the fact that charge collection depends on the depletion layer width.

We see in Table 1 the percentage of charge collected by drift and diffusion. For the lower energy α-particle, these values agree well with simulations [5]. However, for the higher energy α-particle, our data show a lesser amount of diffusion charge collected than that expected. This could be due to the small area of the capacitor, since the amount of charge collected by diffusion depends on the surface collection area [10].

Because of the direct dependence of charge collection on depletion layer width, a structure which will decrease the capacitor depletion layer width such as a Hi-C capacitor structure [11] will decrease the amount of charge collected. In addition, the Hi-C structure has other advantages, such as an increased capacitance and ion implants which could also act as a reflecting barrier [7] to decrease the effect of an α-particle strike.

ACKNOWLEDGEMENTS

The authors would like to thank H. Ishiuchi for his cooperation and help with the measurements. The authors would also like to acknowledge useful discussions with Prof. J. Frey and Dr. E. Murray, and the constant encouragement and support from K. Natori and Y. Nishi.

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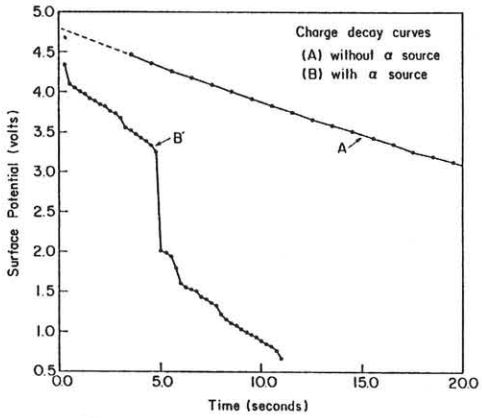

Figure 2. Charge decay curve for a $64\mu^2$ capacitor

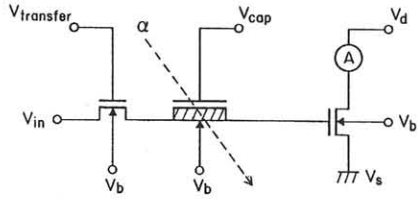

Figure 1. Charge decay test structure equivalent circuit

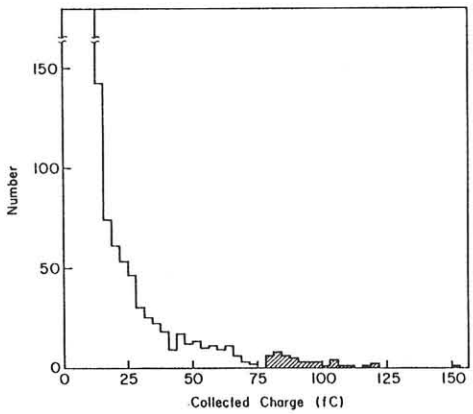

Figure 3. Histogram of charge collected at each measurement time for a $64\mu^2$ capacitor

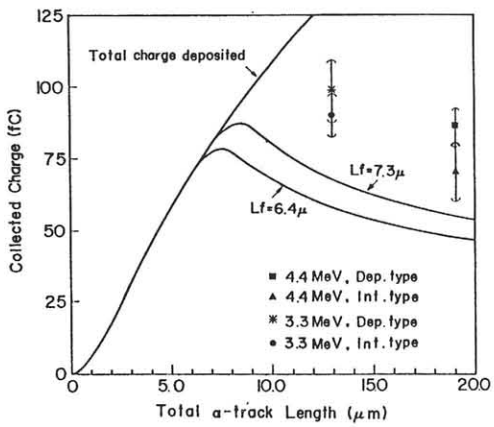

Figure 4. Charge collection as a function of total charge deposited and funneling length. Also shown are MOS capacitor measurement results

α-Energy (MeV)	Capacitor size (μ^2)	Collected charge (fC) Measured	Collected charge (fC) Calculated	% drift	% diffusion
4.4	42(Dep)	86	55	64	36
	64(Int)	70	48	68	32
3.3	42(Dep)	99	68	69	31
	42(Int)	91	59	65	35
	64(Int)	90	59	66	34

Table 1. Summary of calculated and collected charge for the two different energy α-particles
Dep = Depletion type capacitor (with Arsenic implant)
Int = Intrinsic type capacitor (without Arsenic implant)