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Three Dimensional Leakage Current in Corrugated Capacitor Cells

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The mechanism of three-dimensional leakage current in a corrugated capacitor cell for megabit DRAMs has been clarified both experimentally and theoretically using a 3-D device simulator(CADDETH). This study shows that this current is almost completely defined by using the minimum value V_{bi} of the potential barrier height between cells in the simple relationship: $I_L \propto \exp(-qV_{bi}/kT)$. This is the case even if there is a complicated potential form due to three-dimensional effects and/or sophisticated device structures. Furthermore, the three-dimensional effects in the leakage current caused by back bias penetration are discussed in detail. On the basis of these results, significant guidelines are proposed for trench capacitor cells.

§1. INTRODUCTION

Three dimensional device structures and their effects on performance and reliability are becoming major concerns as VLSI technology develops finer geometries. Recently, three dimensional cell structures have been proposed for megabit DRAMs such as trench capacitor(1-2) and stacked capacitor cells(3-4), in order to obtain an adequate signal level and higher soft error immunity. However, three-dimensional effects on leakage current(5-6), and alpha-particle induced soft errors(7) inherent to these structures are now significant problems that must be resolved in memory cell design. Thus, the development of these structures and its associated problems require additional study into the underlying physics of these three-dimensional phenomena.

In this paper, the mechanism of three-dimensional punch-through leakage current is investigated in a corrugated capacitor cell for megabit DRAMs using 3-D simulation(CADDETH)(8) and experimentation. It's scope entails description of 1)key factors dominating leakage current, 2)three-dimensional effects, 3)guidelines for the design and operation of future DRAM cells, and 4) applications.

§2. COMPARISON BETWEEN EXPERIMENTS AND SIMULATION

Simulation and experimentation of leakage current(I_L) were made using cell structures with dimensions as shown in Fig. 1. First, a comparison between experimentation and simulations of leakage current in a corrugated capacitor cell as a function

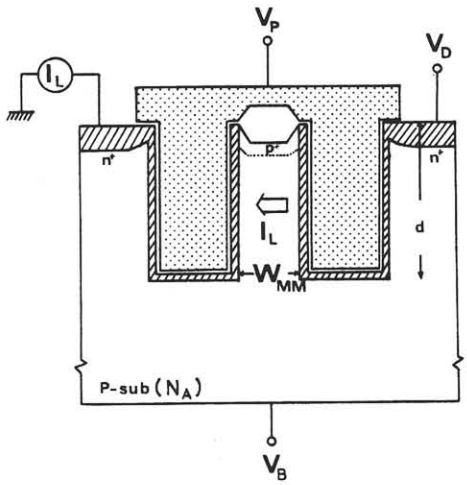


Fig. 1. Cross-section of a corrugated capacitor cell and cell parameters.

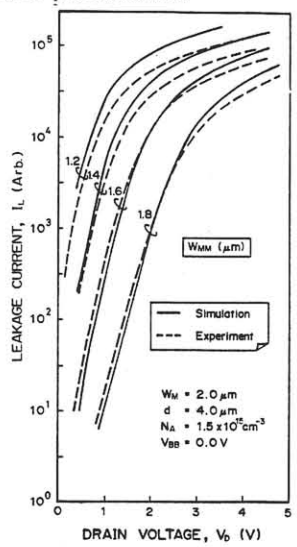


Fig. 2. Comparison between experiments and calculations for leakage current.

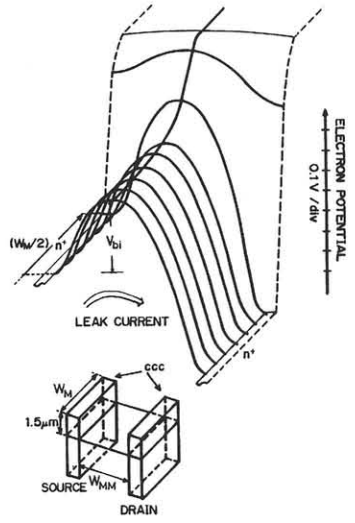


Fig. 3. An example of electron potential between two cells.

of V_D with moat spacing(W_{MM}) as a parameter is shown in Fig. 2. The moat width(W_M) is 2 um and the moat depth(d) is 4 um. It should be noted that the agreement between experimentation and simulation is excellent. Therefore, the mechanism of leakage current can be accurately investigated.

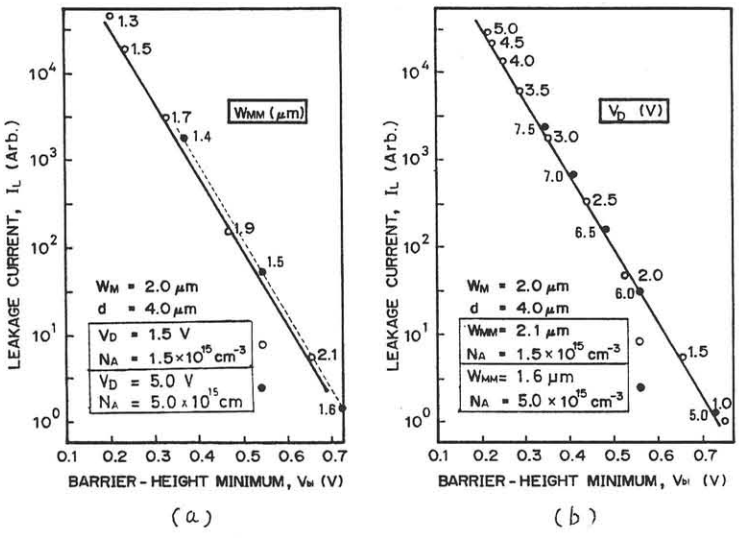
§3. LEAKAGE DOMINANCE BY THE KEY FACTOR(V_{bi})

A typical electron potential form at a depth of 1.5 um in the region between two cells is shown in Fig. 3. Here, W_{MM} = 1.5 um, W_M = 6 um, and V_D= 0.5 V. The barrier height minimum V_{bi} in the potential ridge is defined as shown in this figure. Investigation of the key factor dominating leakage current yields the following simple relationship:

$$I_L \propto \exp(-qV_{bi}/kT) \qquad \cdots\cdots\cdots (3.1)$$

This equation is valid under almost all conditions and cell dimensions: V_D, V_B, substrate impurity(N_A) W_{MM}, W_M, and moat depth(d). Leakage current which flows on the Si-surface is completely suppressed by LOCOS isolation with a proper channel stopper.

As an example, the dependence of the punch-through leakage current on V_{bi} is demonstrated in Fig. 4(a), (b), and (c), using W_{MM}, N_A, and V_D, respectively. Equation(3.1) is very useful in understanding the leakage current mechanism. This relationship is important because the leakage current is determined by the minimum value V_{bi} of barrier height even if a complicated potential structure exists due to three-dimensional effects and/or sophisticated cell structures.



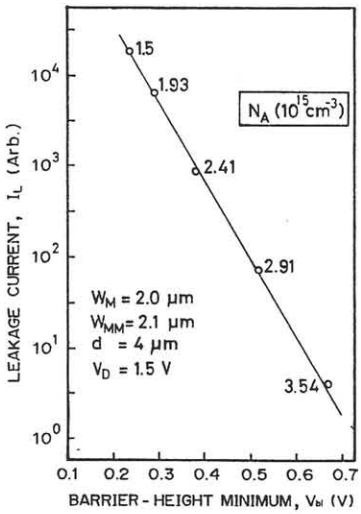


Fig. 4. Dependence of leakage current on V_{bi} with W_{MM}(a), V_D(b), and (c), as parameters.

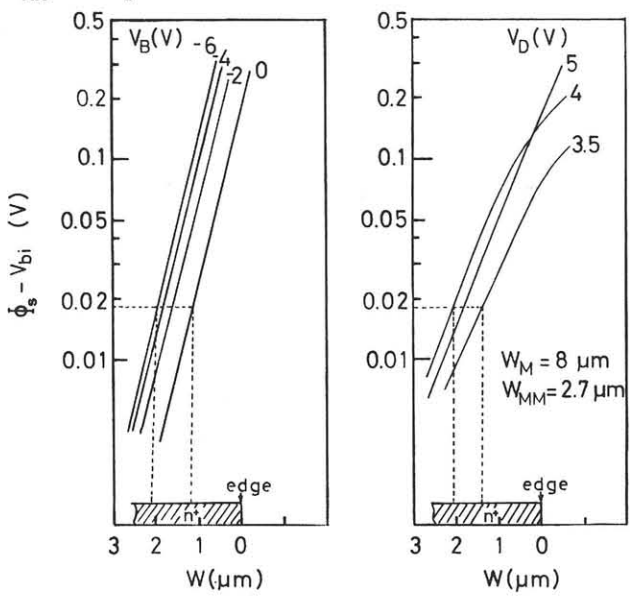


Fig. 5. Potential penetration behavior from a cell edge.

§4. THREE-DIMENSIONAL EFFECTS

Three-dimensional effects of the leakage current appear when cell dimensions(W_M, d) are comparable to the penetration length of the back bias potential(V_B) measured from the moat edge. An example of electron potential penetration behavior from the moat edge is shown in Fig. 5. From this figure, a relationship of the potential Φ_s and the distance W measured from the moat edge is given as:

$$\Phi_s - V_{bi} = A \exp(b \cdot W) \quad \text{..... (4.1)}$$

The slope, b, represents the degree of the penetration, and is strongly dependent on W_{MM} instead of N_A and V_D. In addition, the magnitude,A, depends on V_B.

Three-dimensional effects concerning the moat depth,d, can be discussed in the same way as that of W_M. Based on these considerations, these effects occurs in the region of:

$$W_M < 2W_{MM}, \quad d < W_{MM} \quad \text{..... (4.2)}$$

Of course, these effects can be accounted for by V_{bi} variation. Penetration of the V_B potential a V_{bi} increase, which results in a drastic reduction of the leakage current.

Leakage current is shown as a function of W_M and d in Fig. 6(a) and (b), respectively. A drastic reduction in I_L occurs in the region of W_M < 3 um and d < 1.5 um when W_{MM} = 1.5 um. These three-dimensional effects are sure to provide significant guidelines(5) for cell design.

§5. GUIDELINES FOR TRENCH CELL DESIGN

Considering the dependence of the depletion layer width on N_A, V_D and V_B, two additional relationships are then satisfied under I_L= constant condition:

$$W_{MM} = C_1/\sqrt{N_A} \quad \text{..... (4.3)}$$

$$W_{MM} = C_2\sqrt{V_D + |V_B| + \phi} + C_3 \quad \text{..... (4.4)}$$

where ϕ is the built-in potential. The variable C_3 is a function of W_{MM}. The relationship between W_{MM} and $\sqrt{V_D + |V_B| + \phi}$ in both experimental and calculated terms is shown in Fig. 7.

On the basis of these experiments and calculations two guidelines for reducing the leakage current are established. These are to:

1) cover all side-wall regions of a moat with high-impurity concentrations in order to build a low V_{bi} region.
2) make good use of three-dimensional effects.

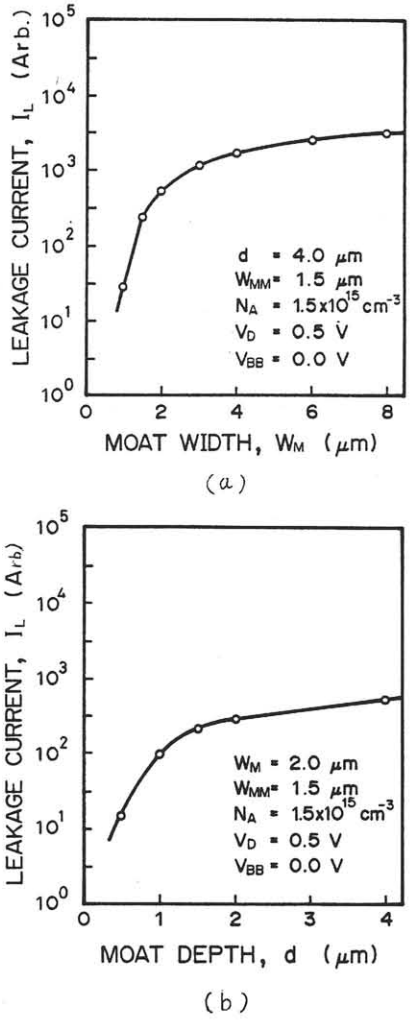


Fig. 6. Leakage current as a function of W_M and d. (Three-dimensional effects)

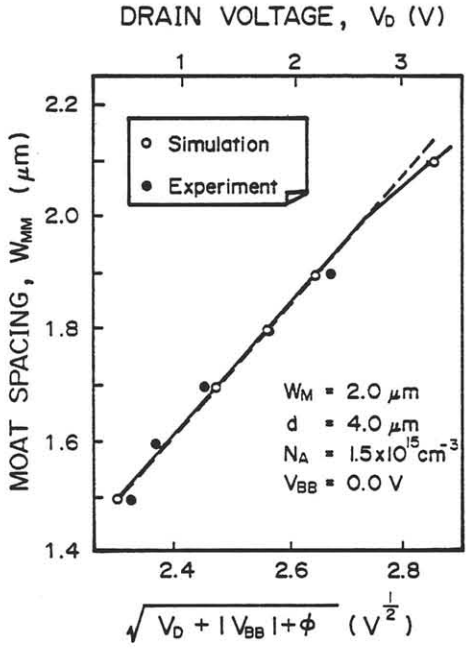


Fig. 7. Relationship between W_{MM} and $\sqrt{V_D + |V_B| + \phi}$

§6. APPLICATIONS

Leakage current in a trench cell with a P(epitaxial layer) on P^+ substrate structure is shown in Fig. 8. The figure shows that a decrease in epitaxial layer thickness is not effective in reducing the leakage current. This is because a part of the low V_{bi} region due to a P-epitaxial region remains. As a result, all the side-wall regions of a moat must be covered with high-impurity concentration layers as shown in the guideline(1). Thus, the use of the "Hi-C" structure, as well as three-dimensional effects, will be indispensable for obtaining good trench capacitor cell scalability.

§7. SUMMARY

The mechanism of three-dimensional punch-through leakage current has been investigated in terms of the minimum potential barrier V_{bi} and three-dimensional effects. It was proven that the leakage current is determined by using V_{bi}, and three-dimensional effects are significant from the viewpoints of cell design and the corresponding physics principles.

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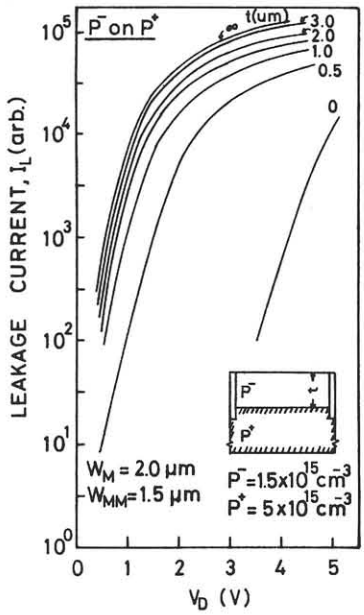

Fig. 8. Leakage current in P on P^+-substrate structure with P^- layer depth(t) as a parameter.

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