Current Leakage Analysis of Folded Capacitor Cell (FCC) for Future Megabit DRAMs

T. HAMAMOTO, N. SHIGYO, K. HIEDA and M. WADA

VLSI Research Center Toshiba Corporation, Kawasaki, Japan

The current leakage characteristics of FCC have been analyzed. At the bottom corner of the trench there is a potential barrier for electron which restricts the current leakage between neighbouring cells. It has been found that this potential barrier is enhanced by forming the p^- region at the trench bottom and applying the substrate bias. The resulting mesa-shaped potential distribution ensures the excellent isolation characteristics of FCC. It has been also found that FCC is effective for isolation spacing as small as 0.5um even in taking the fluctuation of process parameters into consideration.

1. INTRODUCTION

Several new types of DRAM cell have been proposed for use at 4 Mbit, 16 Mbit or beyond. They have in common the use of storage capacitors involving three dimensional structures. The wellknown trench capacitor approach ¹) has presented a difficult problem of charge loss due to the current leakage between neighbouring trenches, and this effectively prevents the reduction of cell to cell spacing below one micron.

The recently developed <u>Folded Capacitor Cell</u> (FCC) ²⁾ not only achieves a very large storage capacitance within a limited cell area, but also exhibits excellent isolation characteristics with minimized isolation spaces in an ideal structure. In this paper, the current leakage flowing between neighbouring cells in FCC has been analyzed with varying process/device parameters. The origin of the superior isolation characteristics of FCC has been clarified and its applicability to ultra high density DRAMs is discussed.

2. FCC STRUCTURE

Figure 1 shows a typical FCC structure. FCC consists of a trench whose side walls are used as storage capacitors. The excellent isolation is achieved by using an oxide partially left at the trench bottom.

The key fabrication steps of FCC are shown in Fig.2. The silicon substrate is grooved by Reactive Ion Etching(a), and boron ions are implanted for device isolation(b). CVD oxide is deposited, then etched back until just enough oxide is left for the isolation between neighbouring cells(c). N⁻ region is then formed by



Fig.1 Typical FCC struture.

solid state diffusion. It is important that the isolation oxide prevents the diffusion of the n⁻ dopant into the isolation region of the trench bottom. Following the formation of the capacitor oxide, a poly Si layer for the cell plate is deposited. Then the gate oxide is formed and the second poly Si layer for transfer gate is deposited. Finally n⁺ layer is formed(d). This process is completely compatible with the <u>Buried Ox</u>ide (BOX) isolation process, which has been successfully used to fabricate a 1M bit DRAM ³.

3. CURRENT LEAKAGE ANALYSIS

Figure 3 shows the FCC structure which are used in the simulation. Current leakage flowing along the trench bottom from the n^- region of Cell-2 to that of Cell-1 is analyzed. The leakage characteristics are influenced by the potential distribution in the isolation region, and the effects of following five parameters on the current leakage and the potential distribution have been investigated:

- (1) hole concentration at the trench bottom (p^{-})
- (2) substrate bias (Vsub)
- (3) spacing between neighbouring cells (S)
- (4) corner radius of the trench bottom (R)
- (5) isolation oxide thickness (Toxf)

The simulated region is indicated by dashdotted line in Fig.3. The current leakage characteristics are obtained by varying the



Fig.2 Key fabrication steps of FCC structure.

Vplate

х

CELL 2

DEPTH

LEAKAGE CURRENT

Vd

nt

CELL I

n

Tox

n+

applied voltage (Vd in Fig.3) to the n^+ region of Cell-2. The parameters listed in Table 1 are used in the caluculation. The device simulation program, TOPMOST ⁴⁾, are used, in which Poisson's equation and the current continuity equation are solved.

Table 1 The parameters used for the caluculation of the leakage characteristics.

| depth of trench | 2 0 | 11m |
|--|------------------------|------|
| isolation spacing | 0.5 | 1100 |
| isolation orido thicknoss | 0.3 | 1100 |
| trench width perpendicular to | 0.5 | um |
| the simulation plane | 2.0 | um |
| capacitor oxide | 100 | A |
| substrate impurity concentration (Psul 2.5x10 |) 215 _{c1} | m-3 |
| surface impurity concentration of n 5.0x10 |) ¹⁹ сі | m-3 |
| junction depth of n | | |
| | 0.2 | um |
| applied voltage to Cell-1 | | |
| applied voltage to plate (Vplate) | 0 | V |
| appried vortage to place (vplace) | 2.5 | V |

3.1 CURRENT LEAKAGE IN IDEAL FCC STRUCTURE

In this section, the current leakage characteristics and their relation to the potential distribution have been analyzed. The corner radius R is set to Oum and the isolation oxide thickness Toxf is set to 0.3um in the ideal FCC structure. The main parameters that dominate the current leakage in FCC are p^- , Vsub and S. Figure 4 shows typical equipotential lines in FCC when Vd is set to 6V and no p^- region is formed.



Fig.3 Structure simulated and the leakage current between neighbouring cells.



In such a structure, electrons flow along the Si/SiO2 interface, where the current leakage is restricted by the potential barrier at the trench corner $^{5)}$. Figure 5 shows the potential along the Si/SiO2 interface as a function of p concentration. When no p region is formed, there is a potential gradient at the trench bottom, which corresponds to the crossing of the equipotential lines to the interface in Fig.4. However, when the p concentration is increased, the absolute value of the potential along the interface increases and the potential gradient disappeares. The resulting mesa-shaped potential distribution indicates that the Vd makes no influence on the potential along the Si/SiO2 interface. The p⁻ concentration of $2 \times 10^{17} \text{cm}^{-3}$ corresponds to an implantation dose of $1 \times 10^{13} \text{cm}^{-2}$. which is about same as the conventional field isolation implantation dose. Taking the n /p junction breakdown into consideration, it is desirable to keep the implantation dose as low as about $1 \times 10^{13} \text{ cm}^{-2}$. Figure 6 shows the potential distribution along the Si/SiO2 interface as a function of Vsub. In the case Vsub is set to -3V, the potential barrier height for electron is about 4.0eV. This barrier height is enough to prevent the current leakage.

Figure 7 shows the dependence of the current leakage on the isolation spacing. When no p⁻ region is formed and Vsub is set to OV, Vd has an influence on the current leakage, especially for small isolation spacing. Under the actual device condition ($p^{-}=2x10^{17}$ cm⁻³, Vsub=-3V), however, the current leakage can be suppressed as low as 10⁻¹⁸ A. It should be noted that the current leakage does not depend at all on isolation spacing down to 0.1um.



Fig.5 The potential along the Si/SiO_2 interface as a function of the p⁻ concentration. The corners of the trench bottom correspond to the distance at 0.3um and 0.8um.



Fig.6 The potential along the Si/SiO₂ interface as a function of the substrate bias.



Fig.7 Effect of the isolation spacing on the current leakage.

3.2 CURRENT LEAKAGE IN PRACTICAL FCC STRUCTURE

In the previous section, the corner radius R is set to Oum and the isolation oxide thickness Toxf is set to 0.3um. But, R and Toxf tend to vary in the practical FCC structure by the process fluctuation. In this section, the dependence of R and Toxf on the current leakage has been investigated. The isolation spacing S is fixed to 0.5um, which is necessary for realizing 16Mbit DRAM.

Figure 8 shows the influence of the corner radius R on the current leakage. The maximum R is 0.25um in practical FCC structure. The current leakage increases about two orders of magnitude when corner radius varies from 0um to 0.25um.



Fig.8 Effect of the corner radius on the current leakage.

Under actual device conditions $(p^{-2x10^{17}cm^{-3}}, Vsub=-3V)$, however, it is suppressed as low as $10^{-18}A$. Its dependence on the corner radius disappears.

The effect of the fluctuation of the isolation oxide thickness Toxf, has also been investigated. Figure 9 shows the relatioship beteween the potential barrier height for electron and the isolation oxide thickness Toxf. The potential barrier height decreases when the oxide thickness becomes less than 0.2um. The n dopant diffuses from the side wall to the trench bottom with decreasing isolation oxide thickness because the junction depth of the n is fixed to 0.2um in this caluculation. In other word, when Toxf becomes less than 0.2um, the potential barrier moves from the corner to the trench bottom, and is likely to be influenced by Vd. It is necessary that the isolation oxide thickness must be large enough to keep the potential barrier existing at the bottom corner of the trench.

4.CONCLUSION

By analyzing the current leakage and its relation to the potential distribution in FCC, following results are obtained. The potential barrier existing at the bottom corner of the trench controls the current leakage characteristics in an ideal FCC. This potential barrier is enhanced by forming the p⁻ region and applying the substrate bias. The resulting mesashaped potential distribution ensures the excellent isolation characteristics in FCC. The fluctuation of the corner curvature and the



Fig.9 Relationship between the potential barrier and the isolation oxide thickness.

isolation oxide thickness is also investigated. It is clarified that the isolation oxide thickness at the trench bottom must be large enough such that the potential barrier exists at the corner of the trench. If these conditions are met in a practical FCC, the current leakage between neighbouring cells can be suppressed even in 0.5um isolation spacing.

ACKNOWLEDGEMENT

The authors wish to thank T. Wada, S. Watanabe, T. Shibata, K. Ohuchi, A. Hojo and H. Iizuka for useful discussions, and to J. Woodhead for his critical reading of this manuscript.

REFERENCES

- 1)H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe and S. Asai, IEEE Trans.Electron Devices, Vol.ED-31, pp. 746-753, 1984.
- 2)M. Wada, K. Hieda and S. Watanabe, IEDM Tech.Dig., pp.244-247, 1984.
- 3)T. Shibata, T. Moriya, K. Kurosawa, T. Mitsuno, K. Okumura, Y. Horiike, K. Yamada and M. Muromachi,IEDM Tech.Dig.,pp.75-78,1984.
- 4)N. Shigyo and R. Dang, IEEE Trans. Electron devices, Vol.ED-32, pp.441-445, 1985.
- 5)S. Goodwin and J. Plummer, IEEE Trans. Electron Device, Vol.ED-31, pp.861-872, 1984.