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# A High S/N Design on Multilevel Storage Dynamic Memory

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A High S/N design is presented of an XY addressed MultiLevel Storage (XY-MLS) 1-Tr dynamic memory circuit. An XY-MLS sense circuit employs both a differential sensing scheme by using a folded data-line structure and charge transfer (C.T.) preamplifier for detecting very small MLS signal voltage. The S/N ratio analysis clarifies that the major causes of S/N degradation are mismatch in storage capacitance $\Delta C_S/C_S$ and leakage charge $Q_L$. Values of $\Delta C_S/C_S<10\%$ and $Q_L<1.5fC$ are required to achieve 4 bits/cell storage. High S/N design will assure four times the density of DRAMs, thus permitting the XY-MLS scheme to fit for the Semiconductor File Memory.

## 1. INTRODUCTION

Recently, demands for faster file memories utilizing semiconductor means have been increasing. One possible approach is to use DRAMs, EEPROMs or SRAMs. This approach, however, suffers from essentially high bit cost compared with magnetic means.

The XY addressed MultiLevel Storage (XY-MLS) scheme has been proposed to realize Semiconductor File Memories[1]. Key features of the XY-MLS are:

(1) usage of standard 1-Tr dynamic memory cells.
(2) MLS signal reading/writing by application of the staircase pulse to the word line.
(3) utilization of the charge transfer (C.T.) preamplifier for accurate sensing of the very small MLS signal voltage.

Density of the XY-MLS memory depends completely on both signal and noise characteristics of the sensing circuit. In this paper, detailed analysis and design on signal to noise ratio in the proposed scheme is made to clarify the limitations. Next, design criteria to establish 4 bits/cell storage or more will be shown. Analytical expressions for signal degradation and noise were successfully developed. Experimental verification of the analyses by using a 4K test memory circuit is also presented.

## 2. CIRCUIT OPERATION

The XY-MLS test circuit is shown in Fig.1. Required sensing accuracy has been realized by the following means:

(1) differential sensing employing a standard folded data-line structure.
(2) signal voltage amplification ($xC_D/C_I$) through signal charge transfer from a data line($C=C_D$) to a sense amplifier input($C=C_I$).

A schematic diagram and observed waveforms of 16 levels/cell storage XY-MLS test circuit operation are shown in Fig.2. During the write operation, a 16-level descending staircase pulse $\phi_X$(j=15,14,---,0) is applied to the word line. The data line voltage is changed from low to high during the intended period of staircase pulse.

During the read operation, a 16-level ascending staircase pulse $\phi_X$(i=0,1,---,15) is applied. Signal charges appearing on the data line are transferred to the sense amplifier (S.A.) input, and are compared with dummy charges. A cross-coupled pair of S.A. detects the sign of the signal voltage $S_{i-j}$ in every staircase step.

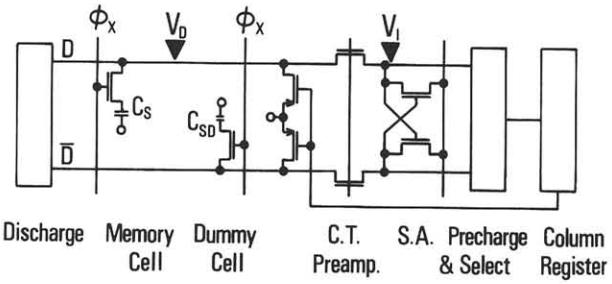



Fig.1 XY-MLS read/write circuit

Thus, sensing accuracy is directly related to signal to noise ratio at the sense amplifier input. $\Delta\phi_X$, $\tau_R$ and $\tau_W$ in Fig.2 denote staircase pulse step, and read and write times, respectively.

## 3. S/N IN XY-MLS MEMORY

### 3.1 Analysis

Memory cell transistors operate under weak inversion conditions during both writing and reading operations. The approximate expression for signal voltage $S_{i-j}$ is shown in Table I. Here, K is the current amplification factor for a single staircase pulse step. Write and read times, $\tau_W$ and $\tau_R$, as well as inverse subthreshold slope $\alpha$ are the major factors in determining the signal voltage $S_{i-j}$. The threshold voltage substrate bias modulation factor $\eta$ also affects the signal.

Device mismatches between a pair of data lines are the major cause of signal degradation. These are:

(1) deviation of half the storage capacitance $C_S/2$ from the dummy cell capacitance $C_{SD}$: $\Delta C_S = C_{SD} - C_S/2$.

(2) mismatch of S.A. input capacitances : $\Delta C_I$.

(3) differences in threshold voltages between a cross-coupled pair : $\Delta V_T$.

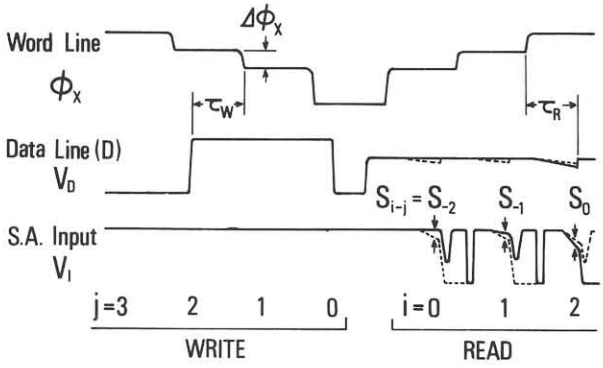
An amount of signal degradation due to $V_T$ mismatch can be minimized and is about $\Delta V_T$, when the S.A. operation speed is slow[2]. Expressions of signal voltage degradations $S_{i-j}$ are summarized in Table I.

Random fluctuation in the data line voltage has been found and it is attributed to 1/f noise and kTC switching noise in the charge transfer preamplifier[3]. The former is proportional to $C_D/C_I$, while the latter is proportional to $\sqrt{C_D}/C_I$. These expressions are also summarized in Table I. The 1/f noise dominates for practical $C_D$ values. The overall signal to noise ratio is expressed as:

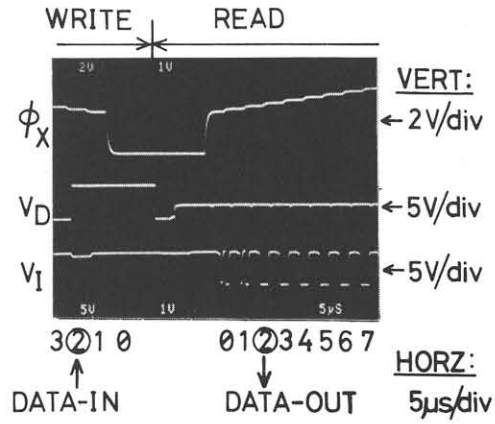
$$\frac{S}{N} = \frac{S_{i-j} - |\Delta S_{i-j}|}{\sqrt{2}\,N} .$$

The S/N ratio is evaluated by measuring detection error rate. The detection error rate $\varepsilon$ is:

$$\varepsilon = \int_{S/N}^{\infty} \exp(-t^2/2)\, dt .$$




(a) Schematic of the operation




(b) Waveforms of the operation in a test circuit

Fig.2 Operation scheme of an XY-MLS circuit

Table I Signal and noise expressions

| | | |
|---|---|---|
| Signal $S_{i-j}$ | | $\frac{1}{1+\eta}\cdot\frac{C_S}{C_I}\left[\alpha\log\left(\frac{\tau_W+\tau_R K_L K^{i-j+2}}{\tau_W+\tau_R K_L K^{i-j+1}}\right)-\frac{1}{2}\Delta\phi_X\right]$ |
| Signal Degradation $\Delta S_{i-j}$ | Storage Cap. Mismatch | $\frac{1}{1+\eta}\cdot\frac{C_S}{C_I}\cdot\Delta\phi_X\cdot\frac{\Delta C_S}{C_S}$ |
| | S.A. Input Cap. Mismatch | $\frac{1}{2}\cdot\frac{1}{1+\eta}\cdot\frac{C_S}{C_I}\left[\alpha\log\left(\frac{\tau_W+\tau_R K_L K^{i-j+2}}{\tau_W+\tau_R K_L K^{i-j+1}}\right)+\frac{1}{2}\Delta\phi_X\right]\cdot\frac{\Delta C_I}{C_I}$ |
| | S.A. $V_T$ Mismatch | $\Delta V_T$ |
| Random Noise from C.T. Preamp. N | $\frac{1}{f}$ Noise | $\frac{q}{C_{ox}}\cdot\sqrt{\frac{n_{Te}\cdot U}{W\cdot L}}\cdot\frac{C_D}{C_I}$ |
| | kTC Noise | $\sqrt{\frac{1}{2}kTC_D}\cdot\frac{1}{C_I}$ |

$K = 10^{\Delta\phi_X/\alpha}$ $\quad$ $C_S$: storage capacitance

$K_L = 10^{Q_L/C_S\cdot\alpha}$ $\quad$ $C_D$: data line capacitance

$C_I$: sense amplifier input capacitance

$\eta$ : $V_T$ substrate bias modulation factor

$C_{OX}$: gate oxide capacitance per unit area

$\alpha$ : inverse subthreshold slope $\quad$ U: constant

$\tau_W$ and $\tau_R$ : write and read time

$n_{Te}$: effective trap density $\quad$ T: temperature

L and W : channel length and width of the C.T. transistor $\quad$ k: Boltzmann's constant

3.2 Experimental verification

Analysis is verified through experiments with a 4K bit XY-MLS test circuit. There is about 17% mismatch in $C_S$ ($\Delta C_S/C_S=0.17$) judging from an observed waveform at the S.A. input of the test circuit. Measured detection error rates are shown in Fig.3. Theoretical error rate dependence on the staircase pulse step $\Delta\phi_X$ is also given in Fig.3, which is calculated with the value of capacitance mismatch $\Delta C_S/C_S=0.17$. Theoretical results are in good agreement with experiments. A staircase pulse step $\Delta\phi_X$ of 110 mV is required to suppress the error rate down to $10^{-20}$ in a test circuit. On the other hand, 60 mV is sufficient if there is no mismatch. Thus, $\Delta C_S/C_S$ minimization is important for high S/N design.

## 4. HIGH S/N DESIGN

Several design criteria to achieve 4 bits/cell storage are shown with a single 5 V power supply. It is assumed that $C_S$=60 fF, $C_D$=0.4 pF and $C_I$=30 fF taking into consideration of the compatibility with DRAMs. Key design parameters for high S/N design are the following.

4.1 The read/write time ratio, $\tau_R/\tau_W$

The effect of $\tau_R/\tau_W$ on S/N ratio is shown in Fig.4. If $\tau_R/\tau_W>1$, signal voltage $S_{-1}$ is degraded because the signal charge flows out prior to the intended timing. On the other hand, if $\tau_R/\tau_W<1$, $S_0$ is degraded because signal charge does not flow out at the intended timing. The optimum condition is $\tau_R=\tau_W$, which gives an S/N ratio of 140. An S/N ratio of 9.3 is required to suppress the error rate down to $10^{-20}$. Consequently a margin of 130 can exist for signal degradation. If there is an 10% deviation in $\tau_R/\tau_W$, it results in an S/N degradation of about 3.3. So, the $\tau_R/\tau_W$ deviation is not the major cause of degradation.

4.2 Device mismatches

The effect of capacitance mismatch on S/N is shown in Fig.5. Here $\tau_R/\tau_W$=1.1 is assumed. Storage capacitance mismatch $\Delta C_S/C_S$ affects the signal twice as much as that of the

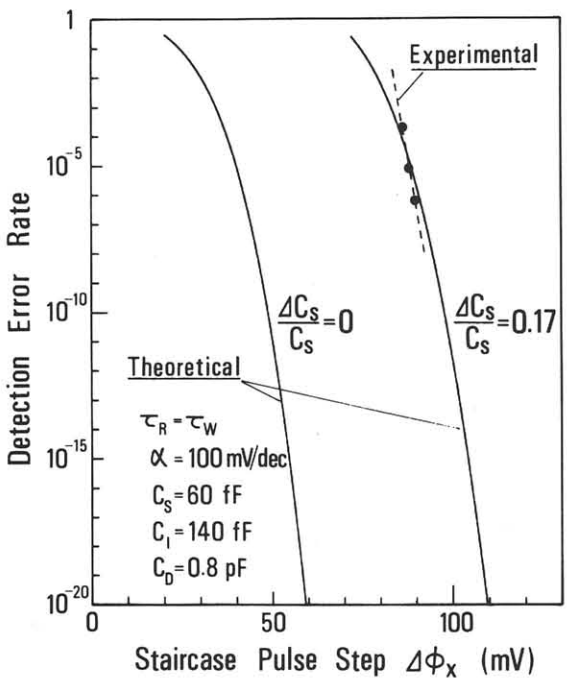



Fig.3 Calculated and experimental detection error rates as functions of $\Delta\phi_X$

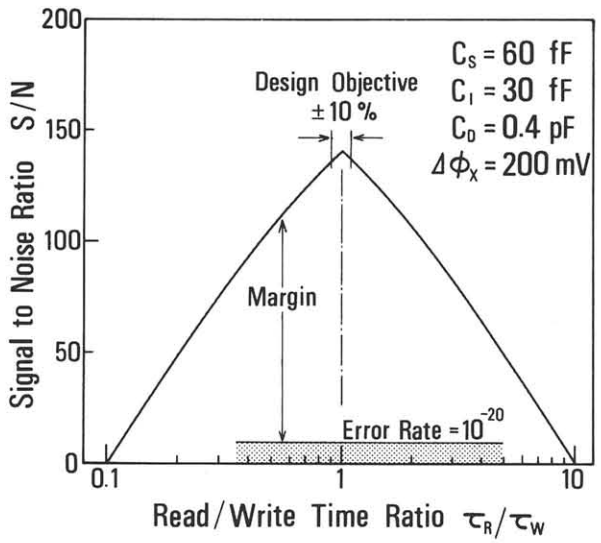



Fig.4 S/N dependence on read/write time ratio

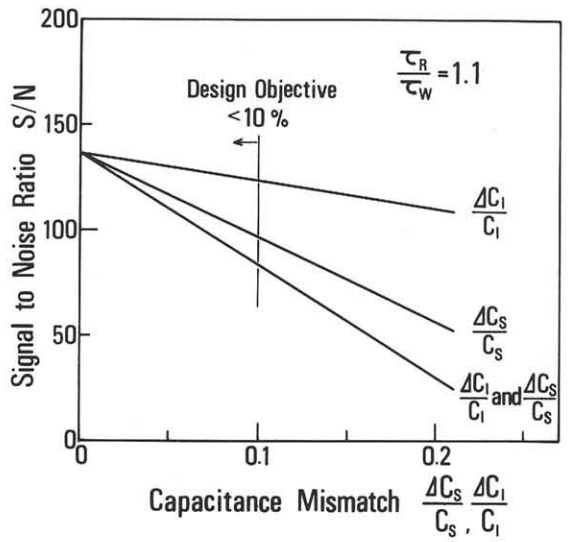



Fig.5 S/N dependence on capacitance mismatch

S.A. input capacitance $\Delta C_I/C_I$. Both $\Delta C_S/C_S$ and $\Delta C_I/C_I$ should be less than 0.1 to suppress S/N degradation less than 50.

Additionally, $V_T$ mismatch $\Delta V_T$ should be as low as 20 mV to suppress S/N degradation to below 20.

4.3 Leakage charge:$Q_L$

The effect of leakage charge $Q_L$ on S/N is shown in Fig.6. In this calculation $\Delta C_S/C_S=\Delta C_I/C_I=0.1$ are assumed. Assuming that the maximum permissible S/N degradation is 30, the leakage charge $Q_L$ should be less than 1.5 fC.

4.4 Discussion

Worst case S/N degradations as a function of staircase pulse step $\Delta\phi_X$ are shown in Fig.7. Since the worst case S/N ratio is expected more than 30, 4 bits/cell storage is feasible through optimum designs presented here. This figure also shows that both storage capacitance mismatch and leakage charge are the major causes of S/N degradations.

If it is realized that $\Delta C_S/C_S=\Delta C_I/C_I<0.05$, $\Delta V_T<10$ mV and $Q_L<0.5$ fC, 5 bits/cell storage is achievable. Design objectives are summarized in Table II.

## 5. CONCLUSION

Analysis and design on signal to noise ratio in the XY addressed MultiLevel Storage scheme has been presented. The formulation of signal to noise ratio has been derived and verified through experimentation. The key factors in high S/N design are reduction of both storage capacitance mismatch $\Delta C_S/C_S$ and leakage charge $Q_L$. Values of $\Delta C_S/C_S<0.1$ and $Q_L<1.5$ fC are required to achieve a 4 bits/cell storage with 5 V power supply.

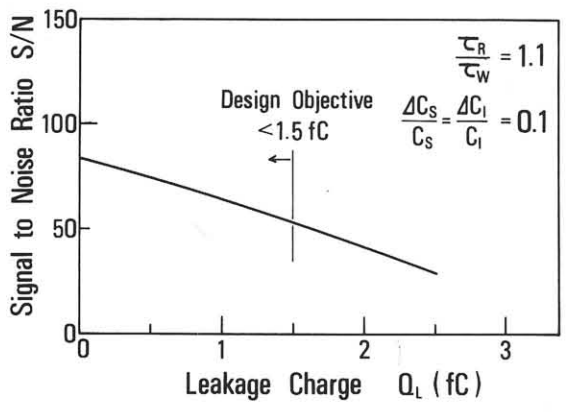



Fig.6 S/N dependence on leakage charge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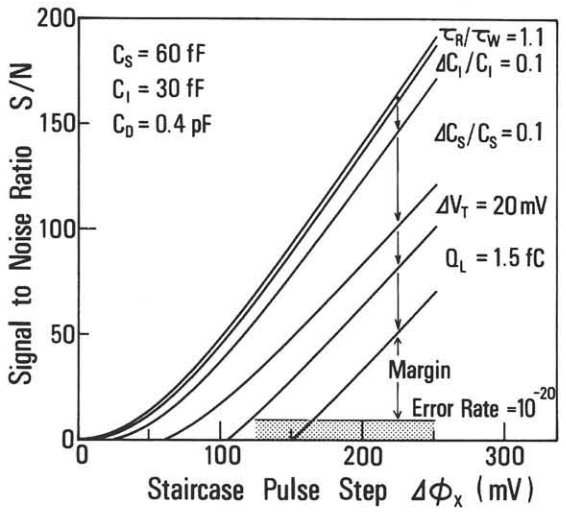


Fig.7 S/N degradation as a function of $\Delta\phi_X$

Table II High S/N design objectives

| | | Test Circuit | High S/N Design | |
|---|---|---|---|---|
| | | | 4 bits/cell | 5 bits/cell |
| Capacitances | $C_S$ | 60 fF | > 60 fF | |
| | $C_I$ | 140 fF | < 30 fF | |
| | $C_D$ | 0.8 pF | < 0.4 pF | |
| Deviation of $\frac{\tau_R}{\tau_W}$ from 1 | | —— | < 10 % | |
| Device Mismatches | $\frac{\Delta C_I}{C_I}, \frac{\Delta C_S}{C_S}$ | $\frac{\Delta C_S}{C_S}\simeq 17$ % | < 10 % | < 5 % |
| | $\Delta V_T$ | —— | < 20 mV | < 10 mV |
| Leakage Charge | $Q_L$ | —— | $\lesssim$ 1.5 fC | $\lesssim$0.5 fC |