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On-Chip Battery Back-Up Circuit for VLSI Static RAM's

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This paper describes a newly proposed circuit for battery back-up control on chip, that is, an On-chip Battery Back-up Circuit (OBBC). Effectiveness of the OBBC is demonstrated through the experiments of separate unit blocks of the circuit and through the integration in an experimental 256Kb six-transistor cell CMOS SRAM. The circuit enables easy realization of nonvolatile memory with high speed write operation and infinite number of write cycle guarantee.

1. Introduction

CMOS SRAM's are widely used with battery back-up mode to provide nonvolatile data storage capability. However, this requires cumbersome external control circuits using several discrete transistors, diodes, and extra board area. To eliminate the difficulty, we propose a battery back-up control circuit integrated on chip, that is, an On-chip Battery Back-up Circuit (OBBC). By the benefit of the circuit, the RAM, combined with very thin battery cells available now, can be used as a nonvolatile memory with high speed write operation and infinite number of write cycle guarantee. This enables the easy realization of word processors, IC cards and other high-performance handheld equipments.

In section 2, basic idea of the OBBC is described. A compa ator and switches which are main parts of the OBBC are evaluated separately in detail.

The OBBC is applied to experimental 256Kb six-transistor cell(6T) CMOS SRAM[1]. The results are shown in section 3. The last section is dedicated for conclusion.

2. Basic Idea of OBBC

The required functions for a battery back-up circuit are as follows : detection of power-failure , prevention of error-writing and supplying battery voltage to memory cells.

The circuit diagram of the OBBC is shown in Fig.1, where, it is depicted in case of p-well process. In this case, external supply voltage is applied between V_{DD} pin and V_{SS} pin, while a battery is between V_{DD} pin and $\overline{CE}_1$ / $V_{SS,batt}$ pin. It is designed that sharing $V_{SS,batt}$ pin with $\overline{CE}$ pin does no harm on the operation. Since the battery pin is common to Chip Enable ($\overline{CE}$ or CE) pin, the pin connection is fully compatible with a standard CMOS SRAM. Of course the OBBC can be realized in case of n-well process and the diagram is almost the same as Fig.1 except that the sign must be exchanged. For example, V_{DD} and V_{SS} must be exchanged.

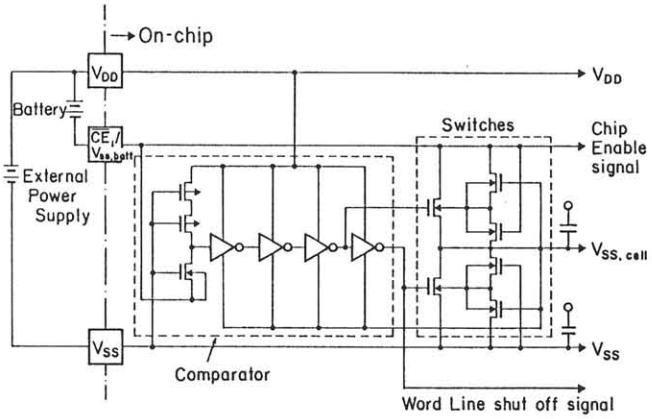


Fig.1 Circuit diagram of On-chip Battery Back-up Circuit (OBBC).

The OBBC is mainly composed of two kinds of circuits, namely a comparator and switches.

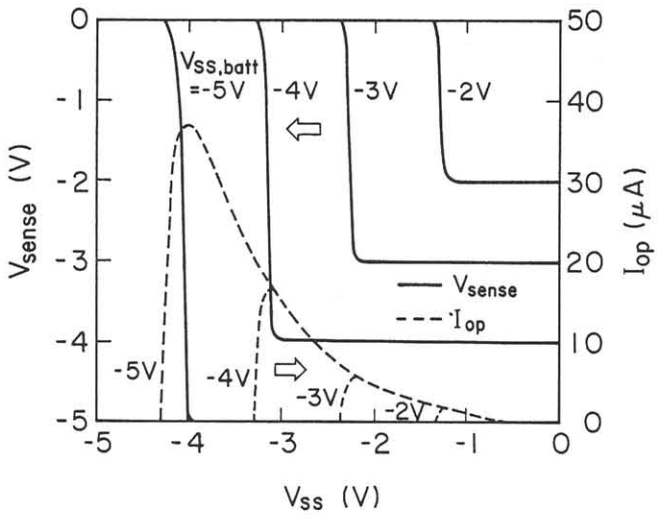


Fig.2 External power fail detection by the comparator.(measured)

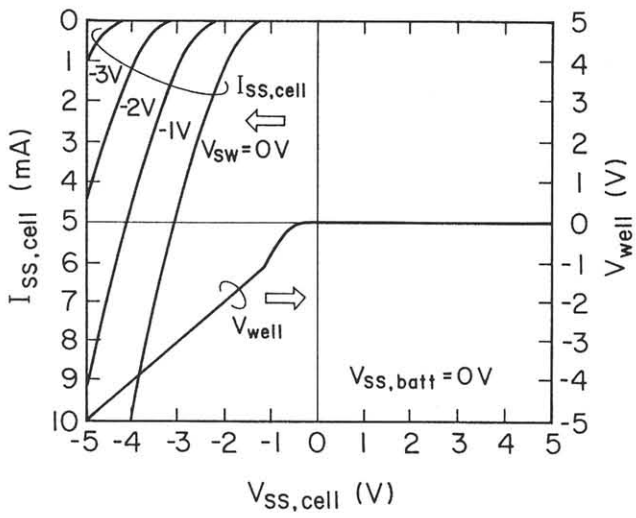


Fig.3 Measured transient behavior of well potential switching circuit.

A comparator, which consists of a sensing part and a buffering part, compares external supply voltage with battery voltage and generates control signals for switches. It also makes word line shut off signal as soon as power-failure takes place. Figure 2 shows measured characteristics of the comparator. Measurement is carried out under the condition that V_{dd} is grounded because V_{DD} is a common line as seen from diagram of Fig. 1. V_{sense} is an output of the sensing part as shown in Fig.1. When V_{ss} rises up from a normal level to a power-failure level and exceeds $V_{SS,batt}+V_{tn}$ (n-ch MOSFET threshold voltage), V_{sense} changes quickly from V_{dd} (zero volt) to $V_{SS,batt}$. External power-failure detection is performed, depending on battery voltage ($V_{SS,batt}$). By the use of the comparator, the OBBC is strong against noise and whatever battery voltage is adapted.

The switches connect an internal power supply line exclusively for memory cells ($V_{SS,cell}$) either to the external supply voltage (V_{SS}) or to the battery ($V_{SS,batt}$). Since this makes a power supply transistor size small, the circuit area of the OBBC can be negligibly small compared with total chip area. P-type well voltage of the switch has to be controlled to prevent the pn-junction of the MOSFET from forward bias during transition from the normal mode to the power-failure mode and vice versa. Therefore, a new well-potential control circuit for the switch is introduced. Figure 3 shows measured characteristics of the switch. As $V_{SS,cell}$ increases from -5v to 0v, V_{well} follows $V_{SS,cell}$ at first and shows a slight kink at the region where two n-channel transistors of a well voltage control circuit are in off state and the well is in floating condition. Even if the well is floated, there is no forward pn-junction current because if the pn-junction is slightly forward and small amount of negative charge is flown into the well, then the well potential is fixed. V_{well} keeps 0v although $V_{SS,cell}$ increases over 0v, which prevents the pn-junction from forward-biased. Figure 3 shows power consumption of the switching circuit. Current flown is only through the switch transistor but not for the well bias circuits. It is demonstrated that V_{well} is properly generated according to $V_{SS,cell}$.

3. Evaluation of OBBC in Experimental 256Kb 6T CMOS SRAM

Six-transistor cell (6T) CMOS SRAM's are widely employed in battery back-up systems because of their low stand-by power. In order to see the effectiveness of the above-mentioned circuits in real devices, The OBBC is applied to experimental 256Kb 6T CMOS SRAM[1]. The RAM was fabricated by using double level aluminum and double poly-silicon layers with deep trench well isolation. This is the world's first realization of the trench isolated ULSI. P-well process is chosen because the influence of parasitic NMOSFET's at the side wall of trench is eliminated by high impurity concentration for the p-well and moreover, an n-epi wafer is superior to a p-epi wafer in respect to crystalization. Figure 4(a) and (b) show photomicrographs of the chip with the OBBC. The circuit area is as small as 0.1 mm^2 using 2μm

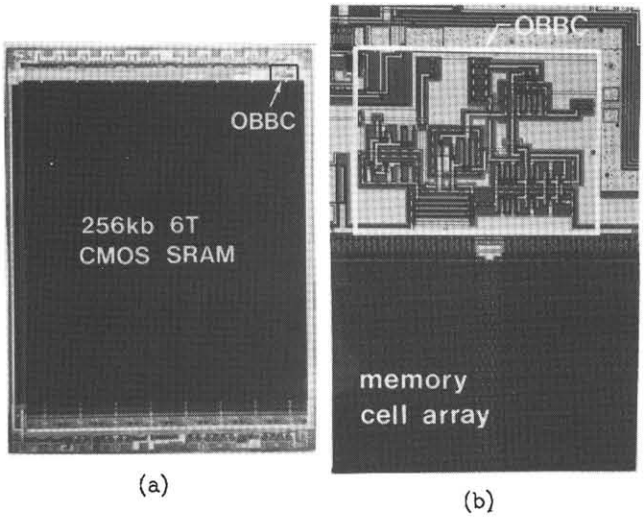


Fig.4 Photomicrographs of the chip with the OBBC.

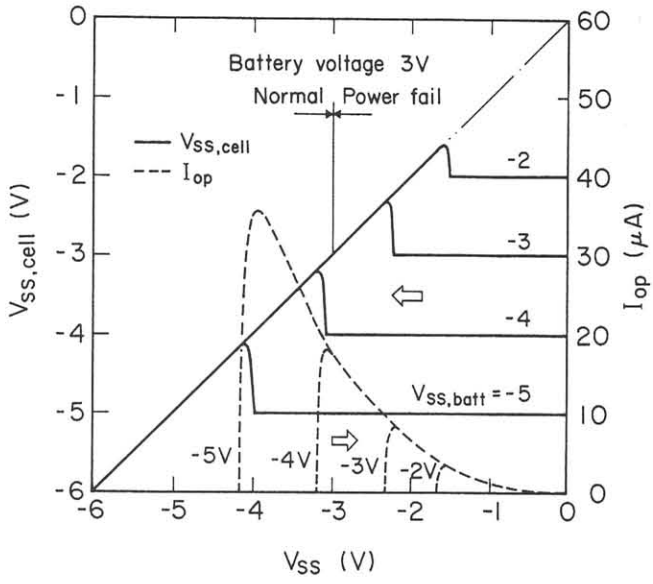
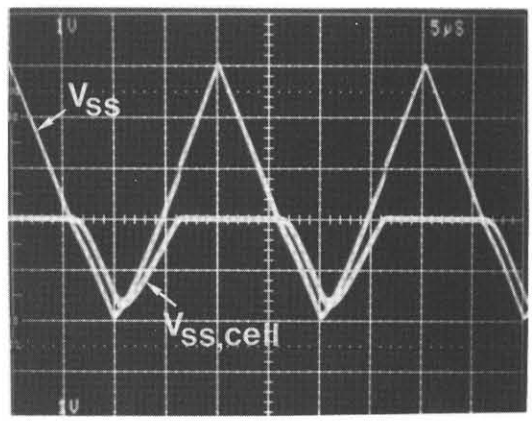


Fig.5 OBBC output ($V_{SS,cell}$) as a function of V_{SS}. V_{DD} is grounded.

design rule, which is less than 0.2% of the total chip area.

The results of the measurement for investigating DC characteristics of the OBBC is shown in Fig.5. The external voltage and the battery voltage are applied to V_{SS} and $V_{SS,batt}$ pins, respectively. The OBBC output ($V_{SS,cell}$), as a function of V_{SS}, indicates the transition from the normal mode to the power-failure mode. Power is consumed by this circuit only during the transition. In the normal mode or in the power-failure mode, no current path exists in the OBBC and hence no power is dissipated. Total current is the same amount of the current in Fig.2, which means that the power consumption of the comparator dominates the total operating power of the OBBC itself.

Figure 6 shows a comparison between measured and simulated AC characteristics. This is a transient behavior of the OBBC output ($V_{SS,cell}$) in response to a lumped external supply voltage. The speed of the power-failure is ordinarily in the order of several micro-second, Therefore, the frequency is chosen to be 20μsec. 3v is chosen as a battery voltage, which is the most popular voltage in battery backup memory systems. The agreement between simulated and measured is satisfactory. Change of the V_{SS} from 0v to -5v corresponds to a power-on while the change from -5v to 0v corresponds to a power-failure. In case of a power-on, voltage applied to memory cells ($V_{SS,cell}$) is the battery voltage ($V_{SS,batt}$) at first but changed to V_{SS}, if an external supply voltage exceeds a battery voltage. A



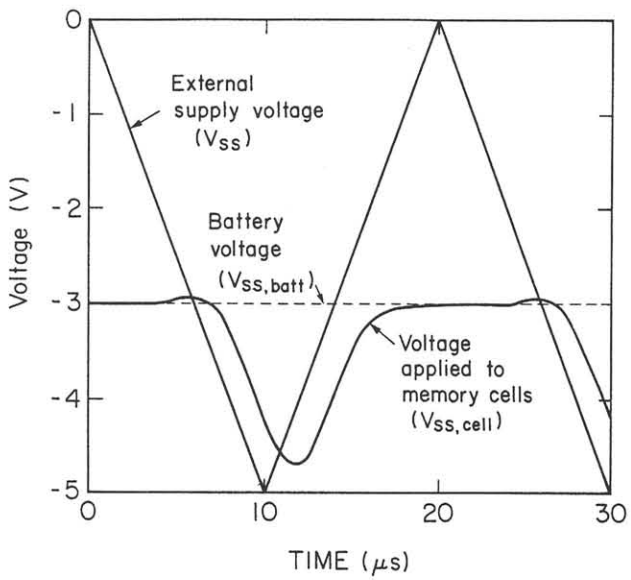


Fig.6 Transient behavior of the OBBC output ($V_{SS,cell}$) in response to a lumped external supply voltage. V_{DD} is grounded. (a) Measured and (b) simulated.

large capacitance between $V_{SS,cell}$ and V_{DD} delays internal supply voltage response. So that, even if an abrupt power-failure occurs, the voltage applied to memory cells is smoothly changed to battery voltage. Non-destructivity of memory storage in switching is experimentally assured.

Lastly load characteristics are shown in Fig.7. Voltage applied to memory cells is displayed as a function of I_{op}, current dissipated in memory cells. Sufficient drive capability for 256Kb memory cell array is demonstrated.

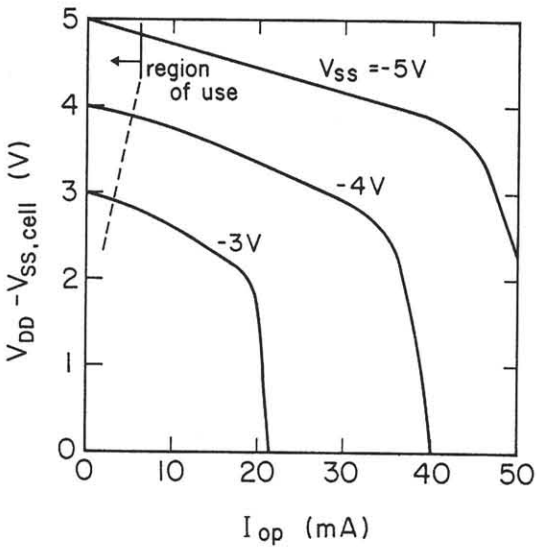


Fig.7 Load characteristics of the OBBC.

4. Conclusion

An On-chip Battery Back-up Circuit (OBBC) for VLSI SRAM's is newly proposed and applied to an Experimental 256Kb 6T CMOS SRAM. Satisfactory battery back-up operation is demonstrated without undesirable influence on normal operation.

Acknowledgments

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Reference

1) K. Hashimoto, Y. Nagakubo, S. Yokogawa, M. Kakumu, M. Kinugawa, K. Sawada, T. Sakurai, M. Isobe, J. Matsunaga, and T. Iizuka, "Deep Trench Well Isolation for 256Kb 6T CMOS Static RAM", 1985 Symp. on VLSI Tech., p.94-95; May, 1985.