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Orientation Controlled SOI by Line-Shaped Laser-Beam Seeded Lateral Epitaxy for CMOS Stacking

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Improvement in seeded lateral epitaxy was achieved through the use of line-shaped laser beam irradiation. The effectiveness of this method was confirmed from the viewpoints of both crystallinity of the laser irradiated layer and characteristics of devices fabricated in the layer. The method was successfully applied to the SOI layer formation on a complex structured substrate for fabrication of a stacked CMOS device, which functioned normally. A 102-stage CMOS inverter-chain fabricated using this method showed a propagation delay time of 700psec/stage.

1. Introduction

The rapid development of SOI (silicon on insulator) structure formation by local heating has attracted great attention as a promising tool for achieving new device structures.

Seeded lateral epitaxy has the advantage over other methods of being able to form crystallographic orientation controlled single-crystal layers¹⁾⁻³⁾ The defined orientation precisely controls orientation dependent properties such as threshold voltage, carrier mobility, oxidation speed The problem of floating substrate which occurs etc. in SOI layers can be reduced by making the layer contact the seeding area.

However, the process still has several problems which need to be settled in the fabrication of stacked devices such as CMOS (Complementary Metal- Oxide-Semiconductor) devices. These are;

- The temperature distribution in the molten Si layer tends to cause crystal growth in a direction opposite to that desired, since the structure of the underlying layer is complex and has spatially distributed various thermal conductivities.
- (2) The poly-Si layer must be melted on both the insulating layer and the single crystal substrate simultaneously. However, the difference in thermal conductivities of the underlying layer makes this difficult. The insulating layer may be made thinner to minimize this difference, but

this would cause thermal damage to the underlying device.

(3) Lateral diffusion of impurities from the seeding region would make the SOI layer an undesired conduction type⁴.

The present paper describes a solution to these problems. Utilization of a line-shaped laser beam⁵⁾ and an optimized capping layer on poly-Si layers enhanced the single crystal growth due to temperature distribution caused by beam suppressing, which is caused in turn by the sample structure. At the same time, only a slight melting of the seeded region was needed for the crystal growth to suppress the lateral diffusion of impurities from the seeding region.

2. SOI formation by linearized laser beam irradiation

SOI formation was achieved by using a CW Ar⁺ laser beam irradiation system, in which the beam was scanned by use of rotating mirrors. Two cylindrical lenses were inserted in the optical path to linearize the circle (Gaussian profiled) beam. The distance between the two lenses was adjusted by monitoring the shape of the molten area on the Si surface and the crystal growth direction. The direction was observed by optical microscope after etching the laser irradiated seedless SOI Secco (poly-Si/SiO2/Si-substrate). structure The most effective laser beam shape to unify crystal growth

direction was found to be a rather elliptical one. This is thought to be due to the heat flow from the edge region of the laser beam during irradiation.

The effectiveness of the linearized beam irradiation was confirmed by evaluating the crystallinity of the seeded lateral epitaxial layer and channel conductance of the MOSFET fabricated in the layer.

of both circular and Optical micrographs laser beam irradiated seeded lateral line-shaped epitaxial layers after Secco etch are shown in Fig.1. The vertical stripe zone in the sample shows the In the case of circular beam seeding area. irradiation, since the crystal growth proceeds normal to the liquid-solid interface, crystal growth almost normal to the beam scanning direction occurred from the beam edge region and terminated crystal growth from the seeding region. Mainly for this reason, the single crystal region was limited to about 10µm from the seed edge.



In contrast, in the case of line-shaped beam irradiation, the liquid-solid interface became straight leading to crystal growth in one direction. As a result, single crystal growth proceeded without any disturbance and single crystal area was seen to increase in size. Thus a single crystal area more than 20µm from the seed edge was obtained.

Comparison of the two beams by evaluating the channel conductance of MOSFET's fabricated in the irradiated layer is shown in Fig.2. In the case of the circular beam, degradation of the conductance occurred in the fabricated n-channel MOS (nMOS) due to the degradation of crystallinity around 10µm from the seed edge, as mentioned above. On the other hand, no such degradation was observed in the pMOS fabricated in the line-shaped beam irradiated region.



Thus the usefulness of the line-shaped beam was confirmed. The method was then applied to the fabrication of stacked CMOS devices.

3. Stacked CMOS fabrication

In the stacked CMOS fabrication, the SOI layer formed was after fabricating an nMOS $(L/W=2\mu m/4\mu m)$, gate oxide thickness: 35nm) on a p-type Si(100) substrate. To preserve a seeding region for SOI formation, the region to be used as a seed was capped with a poly-Si layer, which was formed simultaneously with the nMOS gate electrodes, during As⁺ implantation to form the source and drain region of the nMOS. Otherwise, the implanted the seeding region would diffuse impurities in laterally into the SOI region during the laser-induced melting and solidification processes. After etching off the poly-Si cap, a 700nm-thick SiO₂ layer was deposited by the CVD method on top of the sample which acted as an interlevel insulation layer. The layer was partially removed to define the seeding region, after which a 400nm-thick poly-Si layer which was to be recrystallized was deposited, followed by an encapsulation layer of 60nm-thick CVD SiO, deposition.

The laser irradiation of the poly-Si layer thus deposited on a complex underlying layer was carried out by using the line-shaped beam mentioned above. An optical micrograph of a laser-irradiated poly-Si layer over the nMOS after Secco etching is shown in Fig.3. As can be seen from the figure, the region which was to be used for p-channel MOS (pMOS) active area fabrication contained no grain boundaries in spite of its complex underlying structure.



Fig.3 Optical micrograph of laser recrystallized layer over nMOS in the substrate after Secco etching.

Temperature rise of the poly-Si layer is higher where underlying insulator is thicker. the Therefore, from a simple consideration that the crystal growth proceeds from a lower temperature region to a higher temperature region, the growth proceeds from thin-insulator regions (or regions where there is no insulator i.e. seeding region) to thick-insulator regions. If this actually occurs, as is apparent from Fig.3, the single crystal growth would terminate when it rides over the LOCOS region before proceeding into the active area of pMOS. Even in this case, the above-mentioned area would be single crystallized. However, as the crystal has not grown from the seeding area, crystal orientation of the layer cannot be controlled. As the experimental result shows that continuous crystal growth from the seeding region has occurred, temperature distribution caused by sample structure must have been suppressed by the spatial temperature distribution caused by the laser beam intensity profile.

After removal of the encapsulation layer, P^+ was implanted to make the SOI layer n-type for the fabrication of pMOS. The SOI layer was etched off, leaving the pMOS active area, and the pMOS (L/W=2 μ m/2 μ m, gate oxide thickness; 35nm)

was then fabricated by means of conventional pMOS fabrication process.

An SEM photograph of the cross-section of the fabricated device is shown in Fig.4. It can be seen that the upper pMOS was fabricated on top of the



Fig.4 Cross sectional SEM photograph of the stacked CMOS.

lower nMOS. Even though the process temperature was reduced to 950C after the fabrication of nMOS, the junction depth of the source and drain region was found to be around $0.5\mu m$. This shows the necessity of developing a low temperature process for the fabrication of highly stacked devices.

4. Characteristics of stacked CMOS

I-V characteristics of both the upper pMOS and the lower nMOS with a $2\mu m$ gate are shown in Fig.5. These characteristics confirm the function of both devices; the lower nMOS showing no damage from laser irradiation, and the upper pMOS showing that the recrystallized layers is suitable for device fabrication.

The detailed measurement of the threshold voltage of the nMOS with gate length of 1.4µm showed that there was no noticable deviation between the laser-irradiated and non-irradiated regions. The result indicates that a 700nm-thick interlevel insulation layer was sufficient to protect the underlying devices from laser irradiation damage, and at the same time, as mentioned before, to accomplish seeded lateral epitaxy.

Subthreshold characteristics of the upper pMOS $(L/W=2\mu m/2\mu m)$ are shown in Fig.6. The leakage current in the gate cut-off state was less than 10fA/um at drain voltage of less than -3V, and a tailing factor of 70-80mV/decade was obtained.

A 102-stage inverter chain was fabricated by integrating this stacked CMOS device. Delay time of







(b)

Fig.5 I-V characteristics of the upper pMOS (a) and the lower nMOS (b).





700psec/stage was obtained and it was found that by optimizing the laser irradiation conditions, more than 70% of the inverter chains fabricated functioned normally across a wafer.

5. Conclusion

The usefulness of line-shaped laser beam irradiation on seeded lateral epitaxy was confirmed from the viewpoints of both crystallinity and device The method was successfully applied characteristics. to the fabrication of stacked CMOS devices, in which SOI formation took place on complex substrates. Improvements in this method should make it a crystal tool for obtaining powerful single-crystal orientation-controlled layers on fabrication insulating substrates for the of 3-dimensional LSI's.

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