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Effect of Grain Boundaries on the I-V Characteristics of P-Channel MOSFET/SOI

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This paper reports on the effects of grain boundaries (GBs) on the electrical characteristics of p-channel MOSFETs fabricated in a silicon film on an insulating layer (SOI), for which the direction of GBs are precisely controlled by using the selective laser recrystallization technique.

For GB perpendicular to the current flow, the potential barrier height is measured from the temperature dependence of the device current. This explains the electrical characteristics induced by the presence of GB qualitatively in good agreement with the theoretical expectations. The trap density in GB interface is estimated to be $1.9 \times 10^{12}/cm^2$.

For GB parallel to the current flow, no remarkable effect is found on the I-V characteristics.

1. INTRODUCTION

Grain boundaries (GBs) in the channel region of MOSFETs fabricated in the silicon film on insulator (SOI) have remarkable influence on device characteristics. There have been several reports on the theoretical models of carrier transport and their experimental supports (1,2). However, since GBs were neither perfectly perpendicular nor parallel to the channel direction, and their number in the channel region was not controlled in the conventional laser recrystallized silicon film, experimental data has merely given the rough agreement to theoretical models (1).

In this paper we present the detailed evaluation of GB-effect on the p-channel MOSFET (PMOS) on SOI, which has not been reported yet, in which the direction of GB in the channel region was controlled by using the selective laser recrystallization technique (3,4).

2. SAMPLE PREPARATION

The starting material was 4-inch Si wafer with an 1.1 um thick thermally oxidized silicon dioxide (SiO_2) layer. A 0.5 um thick undoped polysilicon was deposited by LPCVD technique. Impurity doping was performed by phosphorus implantation. The 500 A thick LPCVD silicon nitride (Si_3N_4) was deposited on that material system, and patterned into parallel stripes of 5 um in width and 15 um in center-to-center spacing. The cw argon laser beam of 100 um diameter was rastered parallel to the stripes with a scanning speed and a trace-to-trace stepping of 25 cm/sec and 30 um, respectively. The substrate temperature was kept at 450 C during laser beam irradiation.

Due to the periodical antireflection effect of Si_3N_4, the given heat distribution controlled the grain growth in which the straight GBs were arranged beneath Si_3N_4 stripes, and as a result, 15 um wide single crystal films sandwitched by GBs were obtained. After removing the Si_3N_4 layer, the active region of MOSFETs were defined with aligning their location to the GB-arrangement. The thickness of the gate oxide was 600 A, and the side wall of the device island had additional oxidation cycle in order to avoide the parasitic transistor.

Successive fabrication steps were carried out with a conventional MOS-LSI technology. Figure 1 (a)-(d) show the several conditions of recrystallized silicon islands with and without GB, and the process finished form of PMOS/SOI. The channel dimension used in this study was 4.2 um in length and 7.7 um in width.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 GB perpendicular to the current flow

GB works as a potential barrier for carriers, which is caused by depletion of holes near the GB

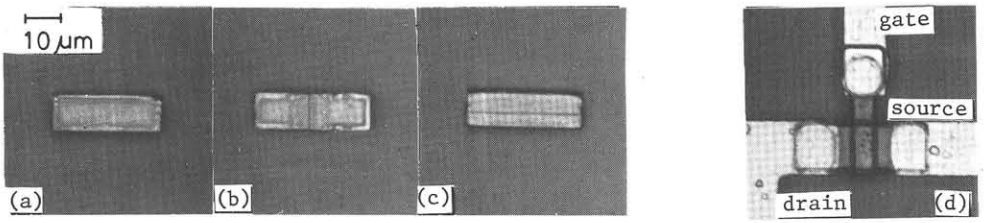

Fig.1 Optical micrographs of recrystallized silicon islands with and without GB, and the process finished PMOS/SOI. The GBs were delinated by secco etching.
(a) no-GB, (b) one-GB perpendicular to channel, (c) one GB parallel to channel, (d) PMOS/FET

due to trapping states at GB interface. Before strong inversion, there are few carriers in the channel to be trapped. Therefore the potential barrier is considered to be small. The maximum height of the potential barrier Ψ_B is given under condition of all the GB states being filled by channel carriers after strong inversion as

$$\Psi_B \simeq \frac{qN_{ST}^2}{8\varepsilon_s \bar{p}} \qquad (1)$$

where N_{ST} is the trap density at GB interface, and $\bar{p}$ is the average hole density in the channel. Since $\bar{p}$ is a function of the gate voltage V_G, Ψ_B also depends on the V_G. And it is also considered that Ψ_B depends on the doping concentration N_D of the channel region. This is because the increasing rate of the average channel carrier concentration as a function of gate voltage for PMOS having the higher doping concentration is higher than that with lower doping concentration.

The current overcoming the potential barrier in the vicinity of GB is given by the classical expression of thermoionic emission (5) as

$$J_T \simeq A^* \cdot T^2 \frac{\bar{p}}{N_V} \cdot \exp\left(-\frac{q\Psi_B}{kT}\right) \cdot \left(\exp\left(\frac{qV_T}{kT}\right) - 1\right) \qquad (2)$$

where A^* is the effective Richardson constant, and N_V is the effective density of states in the valence band. V_T is the voltage drop across the GB region which relates to the drain voltage V_D. If V_T is small, the equation (2) yields

$$J_T \simeq \frac{q\bar{p}A^*}{kN_V} \cdot T \cdot \exp\left(-\frac{q\Psi_B}{kT}\right) \cdot V_T \qquad (3)$$

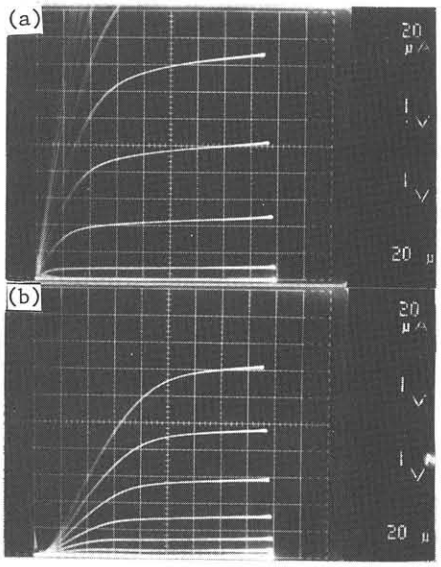

Fig.2 Typical I_D-V_D characteristics.
(a) no-GB, (b) one-GB perpendicular to channel

In order to assess the GB effect on the electrical characteristics expected from above equations (1)-(3), following experiments were performed.

Figure 2-(a) and -(b) show typical I_D-V_D characteristics of PMOS with no-GB and one-GB, respectively. The comparison of them clearly shows reduction of the channel conductance and exponential-like I_D-V_D characteristics of PMOS with one-GB, supporting the equation (2).

The temperature dependence of drain current I_D vs V_G was measured as shown in Fig.3. It was found that the drain current I_D varied sensitively with the temperature for PMOS with one-GB as compared with devices with no-GB. By reducing the drain voltage V_D suitable for equation (3), and plotting the data on log I_D-1/kT form, the potential barrier

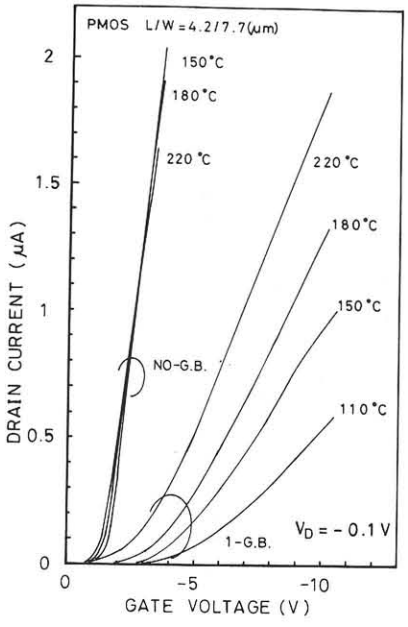

Fig.3 Temperature dependence of the I_D-V_G characteristics.

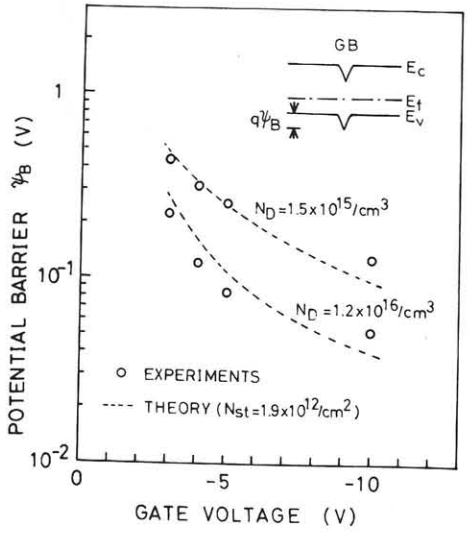

Fig.4 Measured and theoretically calculated potential barrier height.

height Ψ_B depending on the gate voltage V_G was obtained as shown in Fig.4. Although the potential barrier was decreased as the gate voltage became higher, it was found that there remained the potential barrier enough for scattering carriers. This result well explained the lower channel conductance of PMOS with one-GB even under relatively high gate voltage. The increase of threshold voltage for PMOS with one-GB and the softening of the knee of the I_D seen in Fig.3 were also well explained with the presence of the potential barrier, and with its variation depending on the gate voltage.

Maximum values of the potential barrier obtained in this study were 0.46 eV and 0.20 eV, for two samples with doping concentration of $1.5x10^{15}/cm^3$ and $1.2x10^{16}/cm^3$, respectively. The doping concentrations were estimated from the threshold voltages of longer channel devices, since the recrystallized silicon film used in this study had the weak tendency of n-type impurity doping even for samples without phosphorus implantation.

In Fig.4, theoretical curves of the potential barrier on the gate voltage are also shown, that are obtained from the equation (1) using the assumed trap density of $1.9x10^{12}/cm^2$ and average carrier concentration $\overline{p}$ calculated by the 2-carrier and 2-dimensional device simulator. The good agreement of the theory with the experiments indicated that the assumed value was properly consistent as the trap density in GB interface of the laser recrystallized silicon film, and was also in good agreement with the reported value for fine grain polysilicon(6).

Figure 5-(a) and-(b) show the distribution of threshold voltages of PMOS with no-GB and one-GB measured from whole 4 inch wafer, respectively. In

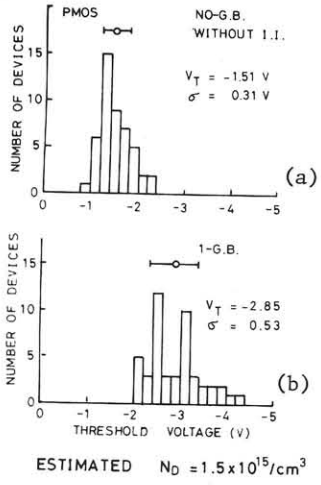

Fig.5 Distribution of measured threshold voltages in a 4-inch wafer from PMOS with (a) no-GB and (b) one-GB perpendicular to channel direction.

addition to the increase of average threshold voltage, the enlarged scattering was found in the PMOS with one-GB as compared with devices with no-GB. This is considered to be mainly due to the trap density in GB interface being not constant from one to another, but depending on the relative misorientation between adjacent crystal grains. Therefore it was indicated that the presence of GB in the channel led to the very poor reproducibility as well as poor controllability of the electrical characteristics of devices.

3.2 GB parallel to the current flow

For GB parallel to the channel direction, measured threshold voltages were almost the same values as the case of no-GB, as shown in Fig.6. And the channel conductance and the leakage current from source to drain of the device with one-GB were in the same level as those of the device without GB. These results indicated that the effective channel length was not altered, and contrasted with the case of n-channel MOSFET/SOI which has suffered from drastic shortening the effective channel length due to fast diffusion of source and drain dopants through GB (7,8). This is considered to be due to the lower diffusivity of boron in GB as compared with the arsenic or phosphorus (9) used in the n-channel devices.

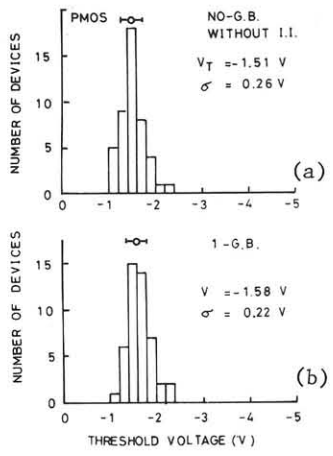

Fig.6 Distribution of measured threshold voltages in a 4-inch wafer from PMOS with (a) no-GB and (b) one-GB parallel to channel direction.

However, since the diffusion constant of boron in polysilicon was reported to be slightly higher than that in single crystalline silicon (10), which implied the fast diffusion through GB, the shorter channel PMOS may have the problem similar to the case of n-channel devices.

4. CONCLUSION

The detailed GB influence on the electrical characteristics of p-channel MOSFET/SOI was investigated, and the obtained results were in good agreement with the theoretical situation. The measured potential barrier well explained the electrical characteristics induced by the presence of GB perpendicular to the current flow qualitatively. The trap density was estimated to be $1.9 \times 10^{12}/cm^2$.

For GB parallel to the current flow, no remarkable effect was found on the electrical characteristics of p-channel MOSFET/SOI.

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