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Fabrication of MOSFET's on Si/CaF_2/Si Structures

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Epitaxial growth of Si/CaF_2/Si structures and characteristics of Si-gate MOSFET's fabricated on Si/CaF_2/Si structures have been investigated. For the growth of overgrown Si film on CaF_2/Si structure, a solid phase epitaxial technique has been successfully applied, to reduce the Ca segregation at the surface of the top Si. In the device fabrication process, relatively low temperature processes(maximum 950°C) have been chosen not to degrade the crystalline quality of the overgrown Si. N-channel and p-channel MOSFET's were fabricated on the Si/CaF_2/Si structures, and MOSFET characteristics were examined. The effective channel mobilities of maximum 570 cm^2/V.sec for n-channel MOSFET and 180 cm^2/V.sec for p-channel MOSFET were obtained for the Si/CaF_2/Si structures. These values were 70 % of those on bulk Si.

INTRODUCTION

Heteroepitaxial growth of Si/insulator/Si structures has potential for formation of silicon on insulator(SOI) devices and three dimensional integrated circuits[1,2,3]. CaF_2 is one of the most promising insulators for these sorts of application, since CaF_2 has a cubic structure which is similar to the diamond structure, and a small lattice mismatch of 0.6 % to Si. In addition, CaF_2 evaporates congruently, avoiding problems with control of film stoichiometry.

Successful epitaxial growth of CaF_2 on Si and Si on CaF_2/Si has been reported by many researchers[4,5,6]. In paticular, Asano and Ishiwara introduced thin amorphous Si deposition prior to the epitaxial growth of Si, which improved the crystalline quality of the Si/CaF_2/Si structure[7]. They have also reported about Al-gate MOSFET's on a Si/CaF_2/Si structure[8]. And another group reported the MISFET's with CaF_2 as a gate insulator[9].

In this presentaion, we discuss the epitaxial growth of Si/CaF_2/Si structures and device performance obtained with Si-gate CMOS process implemented on Si/CaF_2/Si structures. For the growth of the top Si, a solid phase epitaxy (SPE) technique has been applied in order to prevent Ca and F segregation at the surface of the top Si. The device characteristics of SOI-MOSFET's fabricated on Si/CaF_2/Si structures have been examined and compared with those on bulk Si.

EPITAXIAL GROWTH OF Si/CaF_2/Si STRUCTURES

In the present work, we have grown epitaxial CaF_2 layers on Si(100), and Si layers on CaF_2 /Si(100) structures by molecular beam epitaxy (MBE).

Si(100) wafers were stripped in dilute HF and a volatile oxide was grown in a boiled $HCl/H_2O_2/H_2O$ solution. The wafers were then loaded into a MBE system and heated to 850°C for 10 minutes to remove the volatile oxide and impurities. CaF_2 and Si were grown with electron beam evaporators in the MBE system, which has a basic pressure in the 10^{-8} Pa range. 200 nm of CaF_2 was deposited onto the wafers at 610°C. The deposition rate was about 2.5 nm/s. The χ_{min} (channeling minimum yield of back scattering spectrum) of CaF_2 film was 5 %. Wafer temperature was then lowered to less than 100°C and about 3 nm of amorphous Si was deposited. Wafer temperature was elevated again to 560°C-760°C. The rate of temperature rise was controled carefully so as to complete solid phase epitaxial growth of the amorphous Si layer. The crystalline quality of the overgrown Si can be improved by this careful procedure. After the SPE growth of amorphous Si, Si with thickness of 300 - 600 nm was grown by

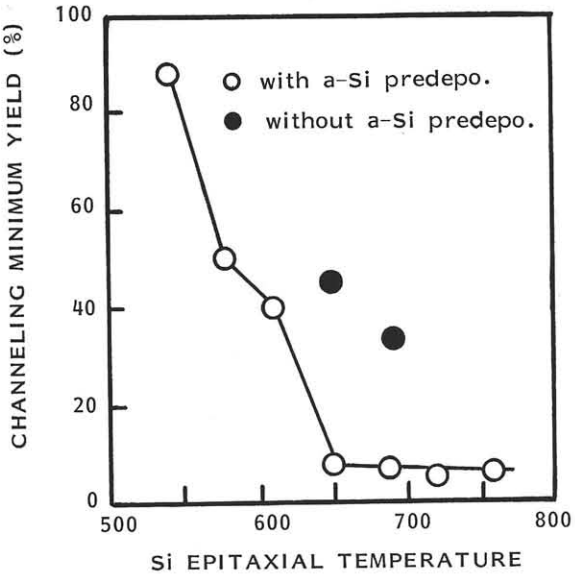

Fig.1 Variation of the channeling minimum yield of $Si/CaF_2/Si$ structures with Si epitaxial temperature.

MBE. The deposition rate was about 0.5 nm/s. The pressure in the chamber was less than $1x10^{-5}$ Pa and $5x10^{-6}$ Pa during the deposition of CaF_2 and Si, respectively.

Fig.1 shows the variation of χ_{min} of the overgrown Si with Si epitaxial temperature. Good crystalline quality of epitaxial Si was obtained at the epitaxial temperature higher than 650°C by using amorphous Si predeposition.

Although the crystalline quality was good, XPS(X-ray photoelectron spectroscopy) and SIMS(Secondary ion mass spectroscopy) measurement revealed that Ca was segregated at the surface of Si. RHEED patterns from the surface of the overgrown Si were not the 2x1 pattern that means a clean Si(100) surface. Different RHEED patterns from the surface of the overgrown Si have been observed with the change in Si epitaxial temperature[10]. For example, Si(100) 6x1 pattern was observed at the epitaxial temperature of 700°C. When different atoms sticked to the clean Si surface, they usually cause the reconstruction of the surface structure. Therefore, we conclude that Ca at the surface of the samples causes the formation of superstructures.

To prevent the Ca segregation, a solid phase epitaxial technique has been applied to the Si overgrowth. After 300 nm of Si growth at 750°C by MBE, wafer temperature was lowered to less than

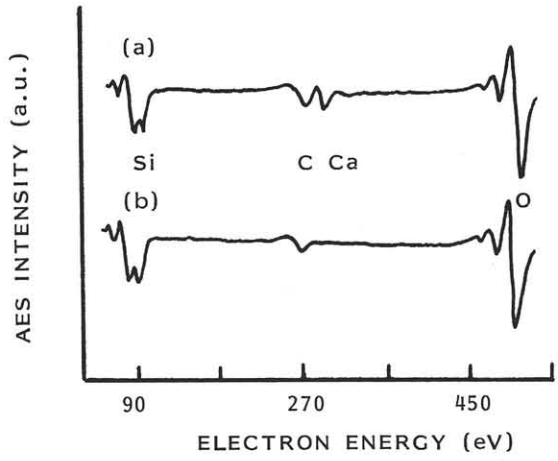

Fig.2 AES spectra from the surface of $Si/CaF_2/Si$ structures grown by MBE(a) and SPE(b).

100°C. Then, 300 nm of amorphous Si was deposited and was crystallized by SPE at about 600°C in the chamber. So the total thickness of epitaxial Si layer was 600 nm. The χ_{min} of the obtained Si epitaxial layer was 8 % and was comparable to that of Si epitaxial layer grown by MBE. RHEED pattern from the surface of Si grown by the SPE process exhibited 2x1 pattern. Fig.2 shows the AES(Auger electron spectroscopy) spectra from the sample grown by MBE process and the SPE process. Although the spectrum(a) from the sample grown by MBE shows the Ca signal, the spectrum(b) from the sample grown by the SPE process has no discernible trace of Ca signal. Thus, it has been shown that the SPE process is useful to prevent the Ca segregation at the surface of the overgrown Si.

DEVICE FABRICATION PROCESS

N-channel and p-channel MOSFET's were fabricated on the $Si/CaF_2/Si$ structures described above. In the fabrication process, Si-gate CMOS process were employed.

The usual Si-gate CMOS process contains several high temperature heat treatments. So, we have investigated the thermal stability of the CaF_2/Si structure and the $Si/CaF_2/Si$ structure[4]. Fig.3 shows the variation of the χ_{min} of CaF_2 and top Si with change in the heat treatment temperature in N_2 ambience for 1 hour. The overgrown Si was not so much degraded even after the annealing up to 1000°C, whereas the intermediate CaF_2 film was degraded by the

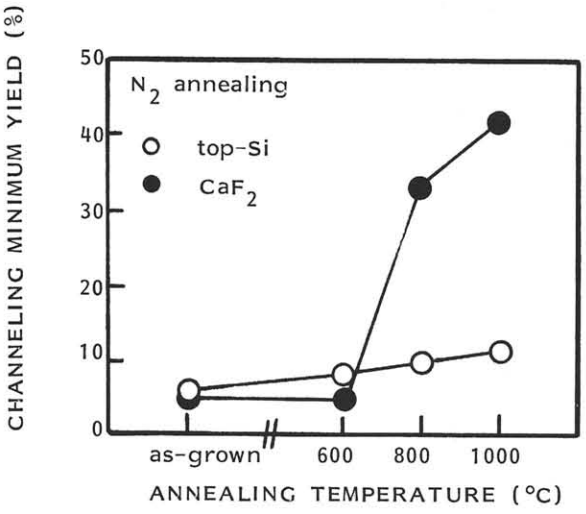

Fig.3 Variation of the channeling minimum yield of $Si/CaF_2/Si$ structures with N_2 annealing temperature.

annealing at temperatures higher than 800°C. Thus, the maximum temperature was chosen to be 950°C in field oxidation at the sacrifice of CaF_2 crystalline quality.

For performing the uniform doping profile without high temperature process, multiple phosphorous implant was carried out with different acceleration voltages to form the N well, and multiple boron implant was also carried out to form the P well. These procedure contains the deep boron implant close to the Si/CaF_2 interface to suppress the back channel leakage current for n-channel MOSFET. A 40 nm gate oxide was grown in wet O_2 ambience and a 400 nm poly crystalline Si was deposited, followed by phosphorous doping step. A 70 KeV phosphorous implant with a $5x10^{15}$ /cm^2 dose and a 40 KeV boron implant with a $1x10^{15}$ /cm^2 dose were carried out for the N^+ and P^+ source drain formation. To compare the FET characteristics, the same FET's were prepared on $Si/CaF_2/Si$ structures and bulk Si wafers.

DEVICE CHARACTERISTICS

Fig.4 shows the typical I-V characteristics of n-channel and p-channel MOSFET's on the present SOI wafers. The channel length and the channel width are 3 μm and 45 μm, respectively. The effective channel mobility of maximum 570 cm^2/V.sec for n-channel MOSFET and 180 cm^2/V.sec for p-channel MOSFET were obtained. These values are about 70 % of those on bulk Si.

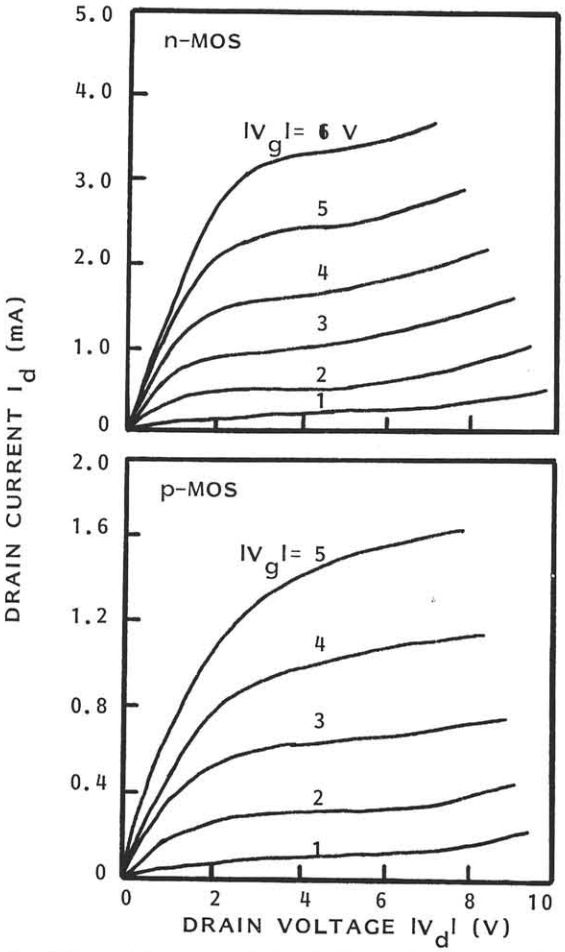

Fig.4 Typical I-V characteristics of n-channel and p-channel MOSFET's fabricated on $Si/CaF_2/Si$ structures.

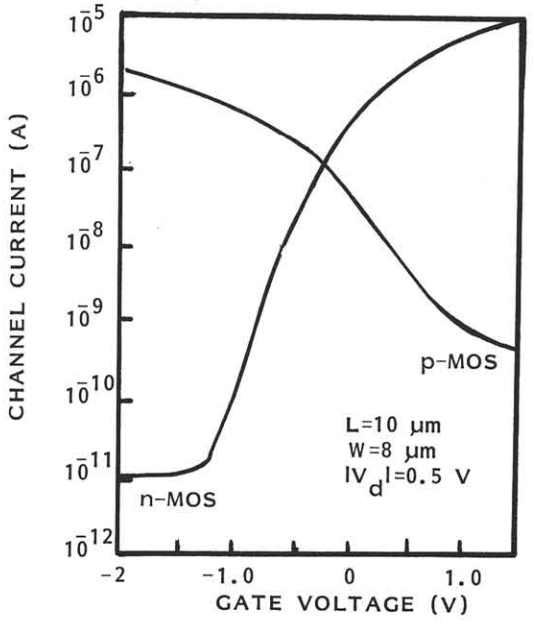

Fig.5 Typical subthreshold channel current of n-channel and p-channel MOSFET's on $Si/CaF_2/Si$ structures.

Fig.5 shows the subthreshold channel current for the n-channel and p-channel MOSFET's on the $Si/CaF_2/Si$ structure. The channel length and the channel width are 10 μm and 8 μm, respectively. These results were obtained at $|V_d| = 0.5$ V. The large current in the vicinity of $V_g = 1$ V for p-channel MOSFET is caused by the drain junction leakage current. The channel stop implant for p-channel MOSFET's was not carried out for this device. Tailing factor ($dV_g/d(\log I_d)$) of about 200 mV/decade was observed for n-channel MOSFET. The value obtained on bulk Si was about 130 mV/decade. The channel mobility and the subthreshold channel current obtained on the $Si/CaF_2/Si$ structure prepared by the SPE process are comparable to those on the $Si/CaF_2/Si$ structure prepared by MBE.

Typical leakage currents obtained on the SOI waferes are large and scattered compared with those on bulk Si. The value obtained on the substrate prepared by the SPE process is one or two orders of magnitude lower than the values on the substrate prepared by MBE.

SUMMARY

We have investigated the epitaxial growth of $Si/CaF_2/Si$ structures and characteristics of Si-gate MOSFET's fabricated on the $Si/CaF_2/Si$ structures. A solid phase epitaxial technique has been applied to the growth of Si film on a CaF_2/Si structure. By the use of this technique, the Ca segregation at the top Si surface has been successfully reduced compared with that of the wafers prepared by molecular beam epitaxy. N-channel and p-channel MOSFET's have been fabricated on the $Si/CaF_2/Si$ structure with relatively low temperature processes (maximum 950°C) which prevent the degradation of the overgrown Si. Characteristics of the MOSFET's were examined. The effective channel mobilities of maximum 570 $cm^2/V.sec$ for n-channel MOSFET and 180 $cm^2/V.sec$ for p-channel MOSFET were obtained. These values were about 70 % of those on bulk Si. The present work indicates that the $Si/CaF_2/Si$ structure has potential for the formation of high-speed and high density SOI devices.

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