

A New Isolation Technology for VLSI

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A new isolation technology, which realizes high packing density of VLSI, has been developed. In this technology, the isolation region is formed by selective oxidation using a unique structure mask. This oxidation mask consists of conventional $\text{Si}_3\text{N}_4/\text{SiO}_2$ mask and thin nitride mask formed at the perimeter of the $\text{Si}_3\text{N}_4/\text{SiO}_2$ mask by self-aligned technique. The submicron isolation region with the width exactly equal to the mask dimension is realized without generating crystalline defects. The device electrical characteristics are equivalent to those of the LOCOS isolated device. The feasibility of this technology has been verified by fabricating a 256 K bit DRAM.

1. INTRODUCTION

Local oxidation of silicon (LOCOS) technology is widely used for LSI isolations. However, in the LOCOS process, a lateral oxidation under the nitride mask, so-called bird's beak, reduces an effective device area and becomes one of the limiting factors in achieving high packing density of VLSI. Recently, several new isolation technologies have been proposed as alternatives for LOCOS.¹⁾⁻⁵⁾

This paper presents a newly developed isolation technology, OSELO (Offset Local Oxidation) for submicron level VLSIs. In this technology, the oxidation mask consists of conventional $\text{Si}_3\text{N}_4/\text{SiO}_2$ mask and thin nitride mask, called the offset nitride, which is formed by self-aligned technique at the perimeter of the $\text{Si}_3\text{N}_4/\text{SiO}_2$ mask and is in direct contact with the silicon surface. This offset nitride plays an important role to shut off lateral oxidant diffusion, and suppress the bird's beak. OSELO has the following advantageous features. (1) No pattern transfer difference between mask and final device geometry, (2) formation of submicron isolation without a decrease in the field oxide thickness, (3) defect free, (4) no additional photomasking steps and (5) compatibility with conventional LSI processing technologies.

In this paper, the OSELO process and the device electrical characteristics are described.

2. FABRICATION PROCESS

The fabrication process of OSELO is explained along with the process sequence shown in Fig.1. (a) 50 nm thermal oxide film (Pad SiO_2) is grown on a 10 ohm p-type (100) CZ silicon wafer. Then, 150 nm LPCVD Si_3N_4 film (Si_3N_4 I) and 300 nm LPCVD SiO_2 film (CVD SiO_2 I) are deposited successively. These films are photoetched using RIE to form the mask for active device areas. (b) 30-100 nm LPCVD Si_3N_4 film (Si_3N_4 II) for the offset nitride and LPCVD SiO_2 film (CVD SiO_2 II) are deposited successively. (c) The anisotropic dry etching is performed to leave CVD SiO_2 II and Si_3N_4 II around the mask. Then, channel stop boron is implanted. (d) Remained CVD SiO_2 I and II are etched off by HF solution. In this manner, the offset nitride is formed self-aligned to the $\text{Si}_3\text{N}_4/\text{SiO}_2$ mask. (e) Selective oxidation is carried out in wet O_2 at 1000 °C.

In this process, the offset nitride width and thickness can be independently controlled by the CVD SiO_2 II and Si_3N_4 II thicknesses, respectively. The offset width is proportional to the CVD SiO_2 II thickness.

Figure 2 shows SEM cross-sectional views of isolation structures formed by the LOCOS and the OSELO processes using the same mask. The offset nitride width and thickness are 240 nm and 50 nm, respectively, and the field oxide thickness is 750 nm. In the LOCOS sample, bird's beaks extend and the isolation width becomes wider than the mask

size. In the OSELO sample, on the other hand, the encroachment of the bird's beak into the active region is completely suppressed by the offset nitride, and the isolation width is the same as the mask size.

3. BIRD'S BEAK EXTENT AND CRYSTALLINE DEFECT

Figure 3 shows the dependence of a bird's beak extent W_B on the offset nitride width w_o . The thickness of the offset nitride is 50 nm. W_B decreases with increasing w_o . W_B becomes zero when w_o exceeds a value which depends on the field oxide thickness T_{ox} . This value is 240 nm for 750 nm thick field oxide and 400 nm for 950 nm thick field oxide. In 550 nm thick field oxide, W_B is zero in the range of w_o from 50 to 240 nm.

The dependence of the bird's beak extent W_B on the offset nitride thickness t_o is shown in Fig.4. The offset width is 240 nm. W_B decreases with increasing t_o . W_B becomes zero when t_o exceeds a value which depends on the field oxide thickness. This value is 50 nm for 750 nm thick field oxide and 70 nm for 950 nm thick field oxide. In 550 nm thick field oxide, W_B is zero in the range of t_o from 30 to 50 nm.

In order to investigate crystalline defects which are generated during the selective oxidation step, the samples were examined by Wright etching and X-ray topography. The generation of crystalline defects was found to be related with the offset nitride thickness. In the samples with the offset nitride thickness in the range of 30 to 70 nm, no crystalline defects were observed. Defects appeared along the mask edge when the offset nitride thickness exceeded 100nm.

Accordingly, in the OSELO process, the encroachment of the bird's beak into the active region is completely suppressed to zero for any field oxide thickness without generating crystalline defects, by choosing the proper combination of the offset nitride width and thickness. For example, 240 nm wide and 50 nm thick offset nitride is available for the field oxide thickness ranging from 550 nm to 750 nm.

4. FIELD OXIDE THICKNESS IN SUBMICRON REGION

One of the advantageous features of the OSELO process over the LOCOS process is shown in Fig.5. This figure shows the dependence of the field

oxide thickness on the final isolation width W_{iso} . In the OSELO process, 240 nm wide and 50 nm thick offset nitride was used. Selective oxidation was carried out for 110 minutes at 1000 °C in wet O_2 to form 550 nm thick field oxide. In the LOCOS process, the field oxide thickness is drastically reduced below the isolation width of 1.3 μm , because of the consumption of oxidant to form the bird's beak.⁶⁾ Therefore, even if the very narrow window mask is used, it is difficult to form the submicron isolation region employing the LOCOS process. In the OSELO process, on the other hand, since the bird's beak is suppressed, the submicron isolation region is formed with little reduction of the field oxide thickness.

5. DEVICE CHARACTERISTICS

Polysilicon gate NMOS devices and p-n junction diodes were fabricated employing the OSELO process. For comparison, the devices were also fabricated employing the LOCOS process using the same masks. In the OSELO process, 240 nm wide and 50 nm thick offset nitride was used. The field boron implantation dose and energy were $3.5 \times 10^{12}/cm^2$ and 75 KeV, respectively. The field oxide thickness was 600 nm, gate oxide thickness was 35 nm and source/drain junction depth was 250 nm.

Figure 6 shows the typical reverse current-voltage characteristics of finger-like p-n junction diodes with 1.8 cm periphery length. The reverse current level of the OSELO sample is as small as that of the LOCOS sample. It means that no crystalline defects are generated.

Figure 7 shows a relationship between the maximum mutual conductance g_m and the channel width W defined by mask. Since g_m is proportional to the effective channel width $W_{eff}(=W-\Delta W)$ where ΔW is the channel width shrinkage, the extrapolated value of the measured points to the abscissa gives ΔW . As can be seen from Fig.7, ΔW of the LOCOS sample is 0.7 μm , whereas that of the OSELO sample is zero, which means that the channel width is exactly the same as the mask size.

The narrow channel effect on the threshold voltage is shown in Fig.8. The threshold voltage of the LOCOS sample drastically increases in the region of the channel width below 2 μm due to a large ΔW . On the other hand, in the OSELO sample, the narrow channel effect is alleviated, which

results in better control for the threshold voltage.

Figure 9 shows the subthreshold characteristics of the active MOSFETs. The subthreshold slope of the OSELO sample is the same as that of the LOCOS sample, and no "hump"²⁾ is observed.

The threshold voltage of a parasitic field transistor of the OSELO sample is shown in Fig.10 as a function of the isolation width Wiso. The threshold voltage decreases in the region of Wiso below 1.5 μm because of the short channel effect. However, even for Wiso equal to 1.0 μm , the threshold voltage is 10 V which is sufficiently high for VLSI circuits. In addition, the short channel effect is expected to be alleviated by optimizing the field implantation conditions and/or making the junction depth shallower. Therefore, from Fig.5 and 10, OSELO is promising for submicron isolation.

The practical feasibility of the OSELO process for VLSI was successfully verified by fabricating a 256 K bit DRAM. The memory cell retention characteristics were equivalent to those of the LOCOS sample. Production yield of the OSELO sample was comparable to that of the LOCOS sample.

6. CONCLUSION

A new isolation technology, OSELO has been developed. In the OSELO process, the isolation width is exactly the same as the mask size and no crystalline defects are induced. Moreover, the submicron isolation region is formed without a decrease in the field oxide thickness. The device electrical characteristics of the OSELO sample are equivalent to those of the LOCOS sample. The feasibility of the OSELO process has been verified by fabricating a 256 K bit DRAM. These results demonstrate that the OSELO isolation process is promising for submicron VLSI production.

ACKNOWLEDGMENT

The authors wish to express their appreciations to Y.Kosa and Y.Kawamoto for their encouragement and helpful discussions.

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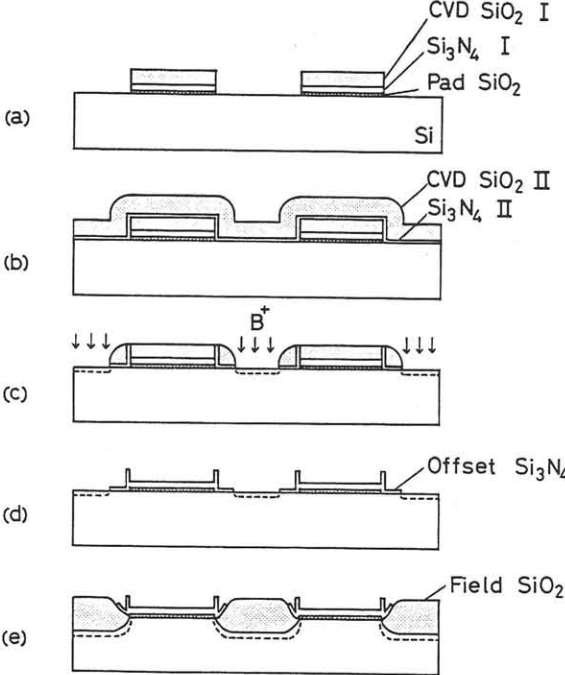


Fig.1 Fabrication process steps of OSELO.

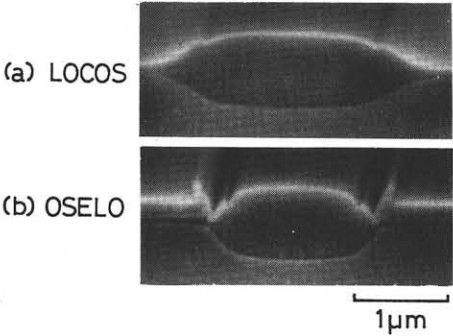


Fig.2 SEM cross-sectional views of isolation structures.

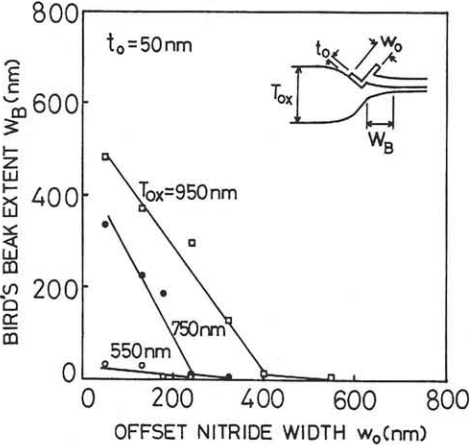


Fig.3 Bird's beak extent as a function of the offset nitride width with field oxide thickness T_{ox} as a parameter.

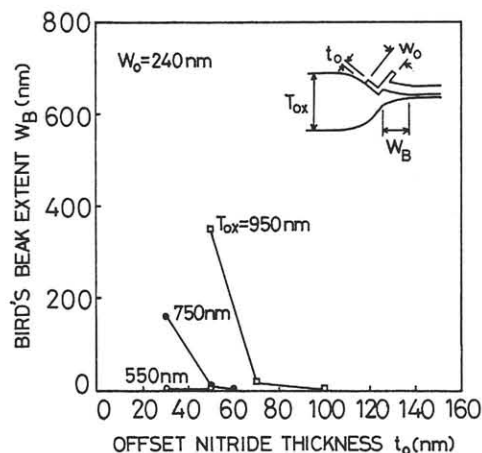


Fig.4 Bird's beak extent as a function of the offset nitride thickness with field oxide thickness T_{ox} as a parameter.

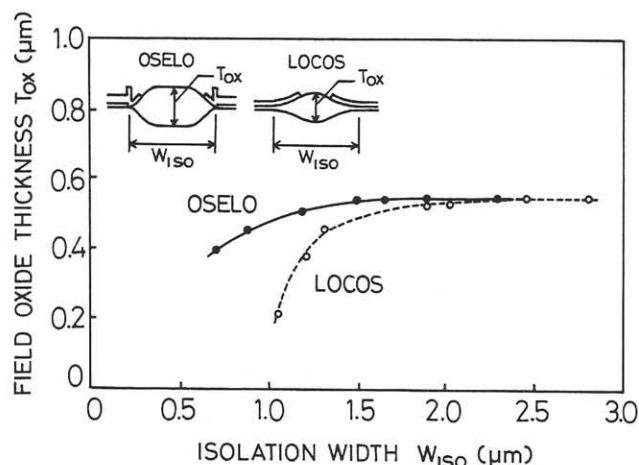


Fig.5 Field oxide thickness as a function of isolation width.

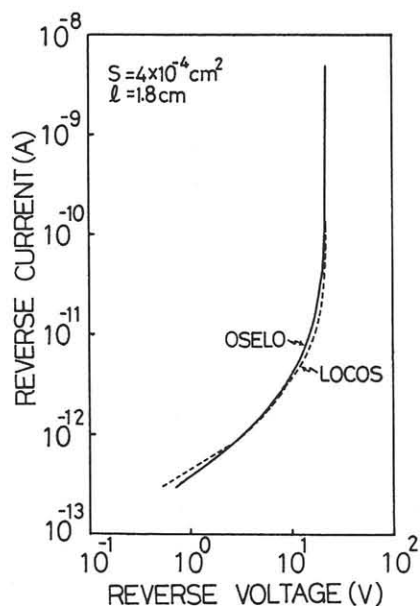


Fig.6 Reverse current-voltage characteristics of p-n junction diodes.

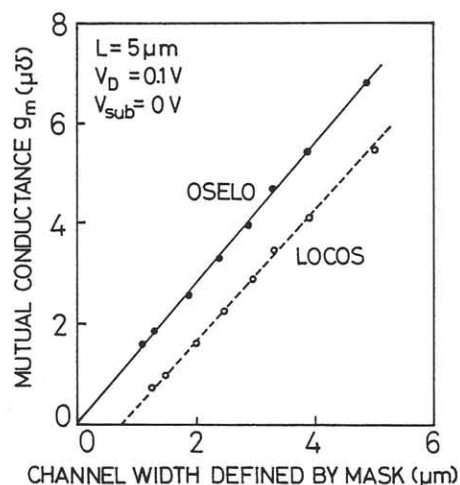


Fig.7 Mutual conductance as a function of channel width defined by mask.

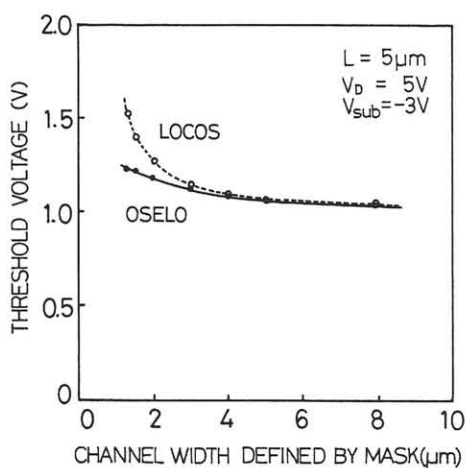


Fig.8 Threshold voltage as a function of channel width defined by mask.

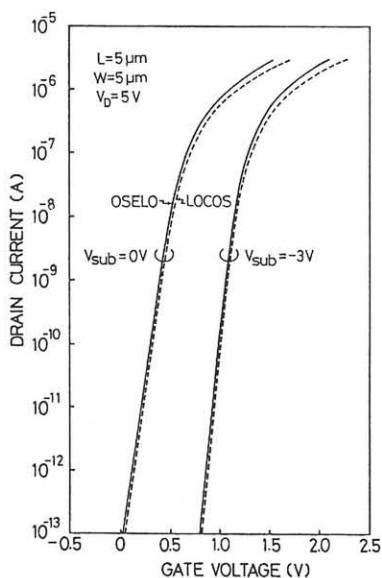


Fig.9 Subthreshold characteristics of active MOSFETs.

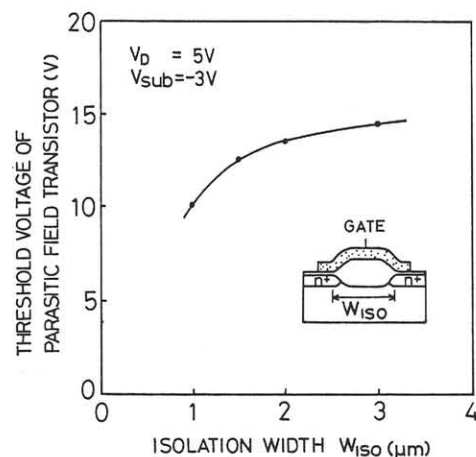


Fig.10 Threshold voltage of a parasitic field transistor of the OSELO sample as a function of isolation width.