Extended Abstracts of the 17th Conference on Solid State Devices and Materials, Tokyo, 1985, pp. 345-348

A-5-2

A New Registration Method for Continuously Moving Stage Variably Shaped Electron Beam Systems

T.Ohiwa, M.Goto, R.Yoshikawa, H.Wada, T.Tojo and Y.Muraguchi

VLSI Research Center, Toshiba Corporation

1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan

A new registration method for continuously moving stage e-beam systems has been developed. In this method, the exposure area is divided into 250 μm□ areas, and e-beam drawing positions are corrected for each 250 μm□ area. The position correction data are calculated with four registration mark positions, which are located in dicing lines for each chip. For optical reduction projection and e-beam direct writing hybrid lithography, e-beam patterning is adjusted to optical patterning using above method. Distortions due to optical reduction printing are measured by e-beam scanning on optically printed marks. Then, the patterns are directly written on the wafer while correcting both wafer distortion and optical patterning distortion. Accordingly, ±0.10 μm(3σ) overlay error was obtained for e-beam exposure, and ±0.25 μm(3σ) overlay error was obtained for hybrid exposure.

1. Introduction

The optical reduction projection system which is called by "stepper" is going to allow to develop a 4MdRAM device with critical dimension of 0.8 μm. However, in present, what is a practical lithography technology can not be anticipated for a 16MdRAM with 0.5 μm feature which also will appear several years after.

For 0.5 μm delineation technology, three candidates of X-ray, e-beam direct writing and optical lithographies should be investigated intensively. The X-ray lithography has a high resolution capability and a high throughput, while it does not become a practical tool soon, because of membrane mask problems such as pattern accuracy and mechanical stability. The e-beam direct writing has also a drawback of low throughput in spite of the high resolution. On the other hand, the present steady progress on the stepper may be limitted by unpredictable development on large area projection lens which enables us to resolve 0.5 μm feature. Thus, in the present situation, the optical/e-beam hybrid lithography, which can compensate each other drawbacks of resolution and throughput, is believed to be a most suitable choice for actual 0.5 μm lithography.

Several experiments on optical/e-beam hybrid lithography have been reported.[1)2)3)] However, pattern distortion due to the optical lithgraphy was not corrected. Therefore, the achieved overlay accuracy was not sufficient for producing 0.5 μm devices.

This paper reports a new registration method developed for continuously moving stage e-beam system,[4)] especially optical/e-beam hybrid lithography.

2. Registration method

The e-beam direct writing system used in this work is a continuously moving stage variably shaped beam raster scan system. The 250 μm wide stripe area from one end of wafer to the other end (frame) is exposed by variably shaped e-beam scanning of 250 μm width in the X direction, during the stage is continuously moved in the Y direction. And the neighboring frames are exposed sequentially like serpentine.

The registration procedure of this e-beam system is as follows. At first, a wafer is aligned coarsely to the fixed position on the wafer-pallet by using a optical microscope out side of the e-beam system. Then the wafer-pallet is loaded on a X-Y stage.

The registration marks are the L shape V grooves which are made by anisotropical etching of silicon, as shown in Fig.1(a). The cross section of V groove is indicated in Fig.1(b). And Fig.1(c) represents the detected backscattered electron signal which is obtained by e-beam scanning on (b) pattern. The e-beam scans the 6 positions in one direction on the mark, shown in Fig.1(a). And signals which are otained by 64 times scanning on the mark at each position are averaged, then a concave bottom of the averaged V signal is calculated, as a central position of V groove indicated by the arrow in Fig.1(b). Subsequently, a registration mark position is obtained by the intersection of central lines for both X and Y directions.

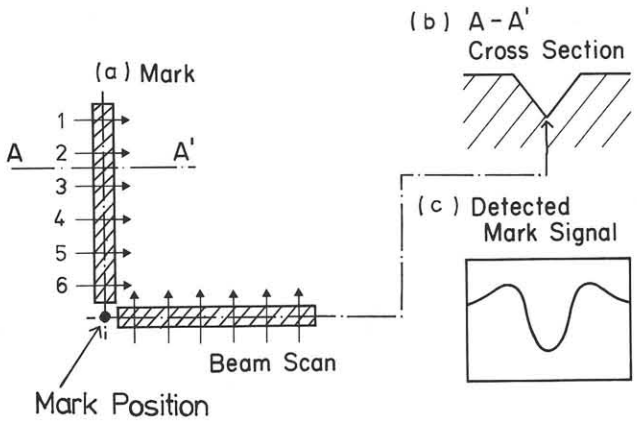

Fig.1 Mark position detection:(a)E-beam scans six positions on the mark in one direction, (b)Cross section of anisotropically etched V groove mark, (c)Detected backscattered electron signal by scanning e-beam on (b) pattern.

Figure 2(a) shows the configuration of wafer fixed on the X-Y stage. And Fig.2(b) indicates the magnified detail representation of the one chip in Fig.2(a). The solid lines represent trapezoidal approximated real chip shape which is deformed from designed chip shape due to mechanical distortion. The registration method composed of two steps are as follows. (1)Wafer registration: Two of the many registration marks which are located in dicing lines for each chip are selected, and the two marks are decteted. Then, the wafer position and the rotation angle toward the stage X-Y axes are obtained, as shown in Fig.2(a). (2)Chip registration[5]: As shown in Fig.2(b), four registration marks located around the each chip pattern area are detected, and the position errors Δ_1~Δ_4 of these marks are obtained. Then the position errors for each 250 $\mu m^{\square}$ area (correction field) which is a division of chip area are calculated with interpolation method, using four mark position errors around the chip.

At e-beam exposure, as shown in Fig.2(a), to overlay the pattern coarsely, the e-beam writing positions on the wafer are shifted by shifting stage position equal to wafer shift, and a frame is exposed along wafer Y axis, during the stage is continuously moved along the stage Y axis. In consequence, the wafer shift and rotation are corrected. And to correct wafer distortion, the e-beam writing position is corrected at each correction field according to calculated postion error data for each correction field, as shown in Fig.2(a). Subsequently, the wafer distortion is corrected. And wafer rotation correction and wafer distortion correction are done independently each other.

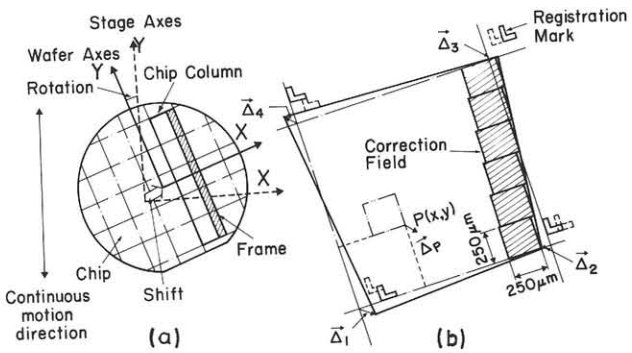

Fig.2 Registration method: (a)The wafer position and rotation angle are determined by position detection of two registration marks.(Wafer registration), (b)Magnified representation of a chip area. The position errors $\Delta 1$~$\Delta 4$ of four registration marks around the chip pattern area, are used to calculate distortion correction data for each 250 $\mu m^{\square}$ correction field. (Chip registration)

This drawing method has been applied to optical/e-beam hybrid exposure, as follows. For hybrid exposure, the stepper distortion is measured by e-beam system, and e-beam writing positions are corrected with these distortion data. Stepper distortion measurement procedure is shown in Fig.3, which is composed of three steps: (a) Distortion measurement pattern exposure

using stepper and formation of V groove marks on the wafer, (b) Mark position detection of distortion measurement pattern, (c) Calculation of stepper distortion and memorizing data. The distortion measurement pattern is the array of registration marks. Stepper distortion data are calculated with mark position data. At hybrid exposure, stepper distortion is corrected using those data in the disk, as shown in Fig.4. The stepper distortion data in the disk are added to registration data, and addion of the two data are used for the exposure. It is expected that e-beam patterning is performed with high overlay accuracy on the optical printed pattern.

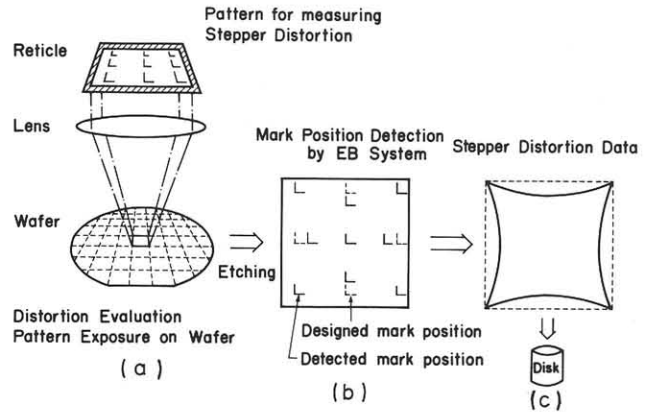

Fig.3 Stepper distortion measurement procedure

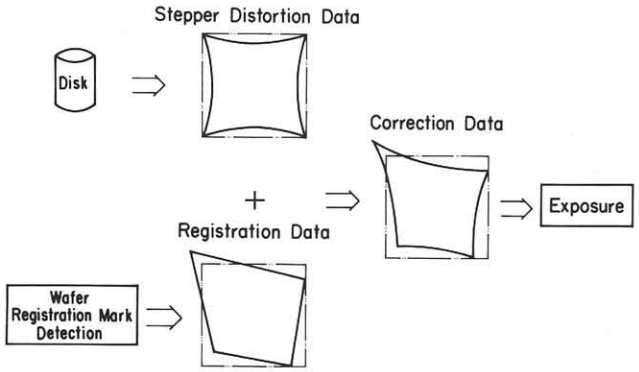

Fig.4 Hybrid exposure distortion correction. Stepper distortion data in the disk are added to registration data and addition of the two data are used for exposure.

3. Stepper distortion measurement

A distortion measurement pattern was exposed with using a ten to one reduction ratio stepper. Stepper distortion, obtained by using our procedure, is shown in Fig.5. It shows pincushion distortion and the maximum distortion is about 0.7 μm. This means that correcting stepper distortion is necessary to improve overlay accuracy for hybrid exposure.

4. Experimental results and discussions

Overlay errors were measured by microscope observation of position error between first layer and second layer of many vernier patterns shown in Fig.6. For e-beam and e-beam exposure, first, the first layer of vernier pattern was exposed after mark detection, nextly the second layer followed the same process, and developed. Then, the overlay error was measured with resist pattern.

For stepper and e-beam hybrid exposure, the first layer of vernier pattern was exposed by stepper and etched to form V grooves. Then, resist was coated on the wafer and the second layer of vernier pattern was exposed by e-beam. After developing, overlay error was measured with resist pattern and Si V groove.

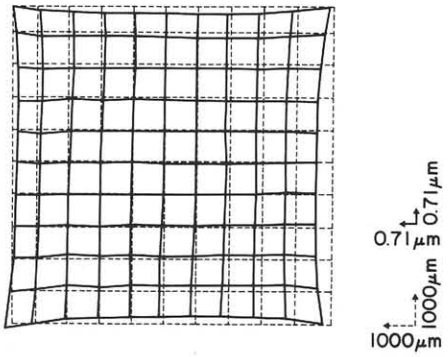

Fig.5 Stepper distortion example. It shows pincushion distortion and maximum distortion is about 0.7 μm.

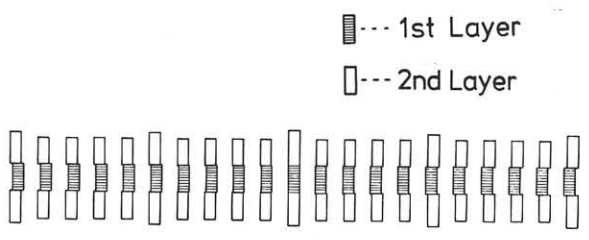

Fig.6 Vernier pattern for overlay evaluation. (0.05 μm / division)

For e-beam and e-beam exposure, less than ±0.1 μm(3σ) overlay error was obtained. It satisfies the accuracy requirement for 0.5 μm VLSI device lithography.

For hybrid exposure, the overlay error within a chip is shown in Fig.7. ±0.25 μm(3σ) overlay error was obtained in the whole wafer. These results show that stepper distortion, shown in Fig.5, is effectively corrected. Obtained overlay error data is equivalent to that for the stepper used in this experiment, but is inferior to that for e-beam exposure. In this method, hybrid exposure overlay accuracy is designed equivalent to that for stepper. Therefore, overlay accuracy for hybrid exposure is improved according to the improvement of stepper overlay accuracy improved. The reason is that the stepper stage positioning error is included in the hybrid exposure overlay error.

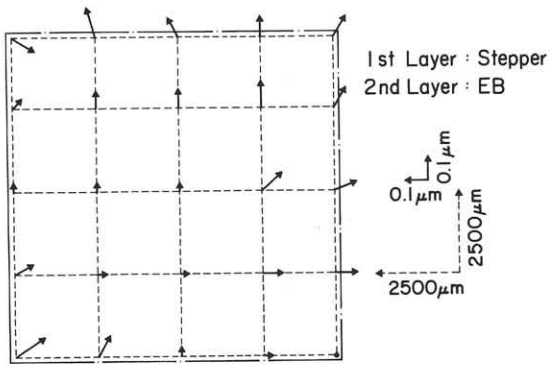

Fig.7 hybrid exposure overlay error within a chip
chip size:10mm*10mm, maximum overlay error:0.25μm

5. Conclusions

A new registration method has been applied to the continuously moving stage e-beam system.

This method has realized the sufficient overlay accuracy for 0.5 μm device fabrication using optical reduction projection and e-beam direct writing hybrid lithography.

Acknowledgments

The authors would like to thank Dr.Y.Horiike and Dr.T.Takigawa for the e-beam system and many helpful discussion and suggestions. We are also grateful to M.Nakase and Y.Kato for their helps with experiments.

1) R.C.Henderson and J.G.Nash, J. Vac. Sci. Technol., 16(6), 1654 (1979)
2) J.C.Potosky, A.J.Higgins, S.T.Hoelke, R.G.Imerson, F.F.Kinoshita, R.L.Maddox and J.P.Reekstin, J. Vac. Sci. Technol., 19(4), 924 (1981)
3) B.J.Lin and T.H.P.Chang, J. Vac. Sci. Technol., 16(6), 1669 (1979)
4) S.Sano, M.Nakasuji, A.Aizaki, H.Wada, M.Ninomiya, F.Chiba and K.Yata, Proceedings of Microcircuit Engineering, 99 (1980)
5) N.Aizaki and M.Nakasuji, Japanese Patent Disclosure 54-118777