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Monolithic Integration of an InGaAs PIN Photodiode, Two InGaAs Column Gate FETs and an InGaAsP Laser for Optical Regeneration

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A monolithically integrated optoelectronic device incorporating an InGaAs PIN photodiode, two InGaAs column gate FETs and a BH laser diode emitting in the 1.3 μm wavelength region is reported. DH/BH epitaxial layers for laser diode and n-InGaAs layer for both PIN photodiode and FET were grown by LPE on SI-InP substrate. A selectively grown n-InGaAs layer with carrier density of about 2×10^{16} cm^{-3} was reproduced. The p-InGaAs layers for FET gate columns and PIN photodiodes were formed by Be-ion implantation and subsequent flash annealing. FET transconductance of about 17 mS and laser threshold current of 25 mA were measured.

INTRODUCTION

Monolithic integration of the laser diode and photodetector with the electronic amplifier paves the way for an optical repeater on a single semiconductor substrate. Thus far, PIN-FET-LD has been reported only in the GaAs/AlGaAs system[1]. On the other hand, InGaAs is the most promising material for high speed long wavelength optical applications, because of its high mobility[2] and wavelength matching with the optical fiber transmission window. A completely planar InGaAs PIN-FET has been developed using a high-purity InGaAs layer and p-column gate FET[3]. Preliminary results of the monolithically integrated PIN-FET-LD are reported, which consists of an InGaAs PIN photodiode, two InGaAs p-column gate FETs and a BH structure laser diode emitting in the 1.3 μm wavelength region. These devices are applicable to optical repeaters as well as optical switching elements[4].

DEVICE DESIGN

The equivalent circuit of the PIN-FET-LD is shown in Fig. 1. Detection and amplification of the input optical signal are performed with an InGaAs PIN-FET which is sensitive up to a 1.6 μm wavelength region. An electrical signal subsequently amplified with another FET is converted into the optical output signal by a laser diode. Fabry-Perot buried structure laser diodes emitting in the 1.3 μm wavelength region were adopted. As shown in Fig. 1, the FETs are connected in a common-source configuration and the n-side of a laser diode is also connected to the FET drain. The n-InGaAs epitaxial layer grown by LPE provides the active layers for both PIN and FET. For simplicity of epitaxial layer growth and the device fabrication process, it is desirable to maintain the same active layer for both PIN photodiode and FET. Therefore, InGaAs layers must be designed in consideration of both PIN and FET characteristics. Because of the optical sensitivity and response speed of the PIN photodiode considered, the carrier density of the InGaAs layer should be as low as possible. On the other hand, carrier density requirements of the FET active layer for high transconductance are opposite to that of the PIN photodiode. In the present design, the carrier density was determined from the requirements on forming the FET gates. The column gate structure was

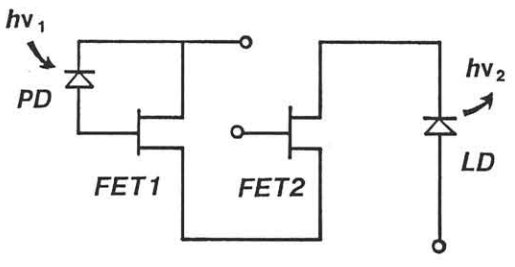

Fig. 1 Equivalent circuit of the PIN-FET-LD.

adopted, because of its moderate requirement on the active layer thickness control. In column gate FETs, cut-off conditions can be controlled by adjusting the gate column spacing. A 2 μm-squared and 2 μm-separated column can be reproduced by the conventional photolithograpy and the following Be-ion implantation. The lateral spread of p-column formed by 200 keV Be-ion implantation and subsequent flash annealing is estimated to be about 0.4 μm. Thus, residual active width between columns is about 1.2 μm. In order to ensure operation in bias voltage level of several volts, the carrier density of the FET active layer must be less than $2x10^{16}$ cm^{-3}. The Be-ion implanted p-layer thickness, after flash annealing, was measured at about 1.2 μm. Therefore, to ensure low gate capacitance and low leak current operation, the FET active layer thickness was designed to be less than 1 μm. In the present device, the FET InGaAs layer thickness is set at about 0.8 μm.

For high quantum PIN photodiode efficiency, an absorbing layer thicker than 3 μm is required. However, an undepleted InGaAs layer produces operation speed deterioration. For several tens MHz range applications, non-electric field layer thickness must be less than 1.5 μm. Low energy Be-ion implantation of 50 keV, used to form p-n junction, produces a p-InGaAs layer of about 0.5 μm thickness. Therefore, the InGaAs layer thickness in regions where PIN photodiodes are formed must be less than 2.5 μm. The cutaway view of the fabricated PIN-FET-LD is shown in Fig. 2. The PIN photodiode is located in the center of the first FET and its sensitive area diameter is 80 μm. The PIN p-electrode is connected with the FET gate. The first and second stage FET have about 280 and 190 columns, respectively. The laser diode cavity length is about 330 μm.

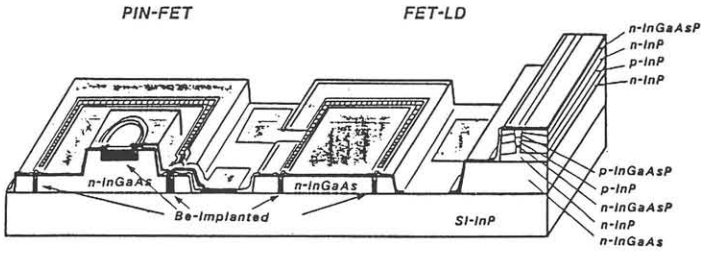

Fig. 2 Cutaway view of the PIN-FET-LD.

DEVICE FABRICATION

Epitaxial layers were grown on a SI-InP substrate. DH/BH layer growth was first done and then InGaAs layer for both the FET and the PIN photodiode was grown, because the selective growth in wide region is more reproducible than that in narrow region. The first epitaxial growth is n-InGaAsP layer, which serves as the laser diode bottom contact layer. The excess connecting resistance caused by the use of the semi-insulating substrate can be reduced to less than 1 ohm by using the quarternary layer with carrier density greater than 10^{18} cm^{-3} and the thickness greater than 2 μm. DH layers providing laser diode were grown in the following order: n-InP lower cladding layer, undoped InGaAsP active layer, p-InP upper cladding layer, and p-InGaAsP top contact layer. After the DH growth, mesas were etched down in the n-InP layer to form the laser stripe with Br-methanol etchant. BH growth consisting of p-InP, n-InP and n-InGaAsP was done to form buried-hetero-structure. Next, the BH layer and n-InGaAsP lower contact layer were etched off everywhere except in the vicinity of the BH laser mesa. Si_3N_4 film was deposited and then removed in regions where the PIN photodiode and the FETs are to be formed. The exposed SI-InP substrate was then cleaned with the organic solvent and InGaAs epitaxial layer was selectively grown on the surface. A high-purity InGaAs layer can be obtained by using In melt annealing in a flowing H_2 atmosphere[5]. InGaAs carrier density and mobility dependence on baking time is shown in Fig. 3. In the figure, the characteristics of InGaAs epitaxial layer grown on SI-InP substrate are shown, for reference, by open and solid circles. InGaAs layers are purified by increasing the baking time. The double circles show data of selective epitaxy on SI-InP substrate with SiN film covered DH/BH layers. The figure shows that the selective InGaAs epitaxial layer maintain almost the same quality as that of the non-selective or ordinary epitaxy. It may be noted that, as the pre-cleaning process, the organic solvent cleaning is as

effective as the Br-methanol light etching which is ordinarily used.

As mentioned, the InGaAs layer carrier density must be less than $2x10^{16}$ cm^{-3}. Therefore, the InGaAs layer growth was done after In-melt baking for 7 hours at 750 °C. After the epitaxial growth, InGaAs layer thickness is adjusted to be less than 1 μm by chemical etching except in the PIN photodiode region. Subsequent etching down to the SI-InP substrate was done for isolation. To form p-InGaAs layers, Be-ion implantation was used and 2 μm squared windows were etched in the SiN film at the FET gate columns. Double-energy Be-ion implantation of 200 keV with the dosage of $2.5x10^{14}$ cm^{-2} and 50 keV of $5x10^{13}$ cm^{-2} was used. As an implantation mask, 1.3 μm thick photoresist and 0.2 μm thick SiN film were used. On the other hand, a 50 keV and $5x10^{13}$ cm^{-2} implantation condition was used to form a p-InGaAs layer for a PIN photodiode. To avoid compositional change in the crystal surface, a 500 A P-CVD SiN film deposition was made prior to the flash annealing at 600 °C, 15 sec. The resultant pn junction gate column is shaped like cylinder with its bottom in the SI-InP substrate, since the formed p-layer thickness is about 1.2 μm. PIN photodiodes have 0.4 μm thick p-InGaAs layer due to the low energy implantation. The above stated two step (200KeV and 50 KeV) Be-ion implantation is necessary in case of carrier density of around $2x10^{16}$ cm^{-3}.

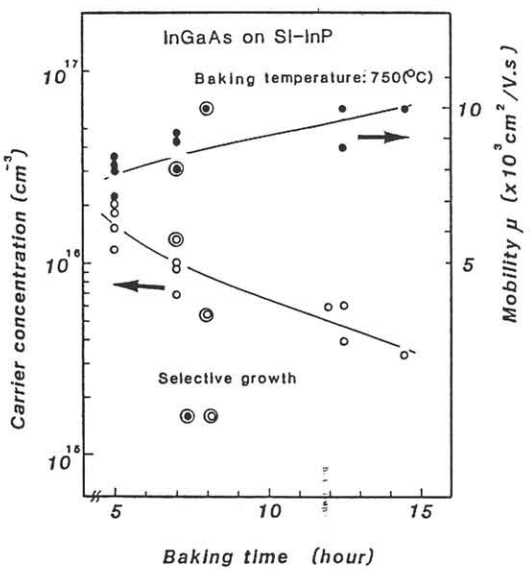

Fig. 3 Effect of baking time on purification of InGaAs layer grown by LPE on a SI-InP substrate. Double circles show data of selective epitaxy, while circles show those of ordinary epitaxy.

This is different from the case of the previously reported PIN-FET[3], in which p-InGaAs layers can be simultaneously formed for both gate column and PIN diode, because in that case high-purity InGaAs layer with carrier density of less than $1x10^{15}$ cm^{-3} was used and thus the active layers between the gate column bottom and the SI-InP substrate were depleted. Contact was made to the Be-implanted region using TiPtAu, while AuGeNi/Au was used to the common and drain n-type electrode.

DEVICE CHARACTERISTICS

Fig. 4 shows the static drain-source current variations of the FETs incorporated in the PIN-FET-LD. The PIN-FET static characteristics yields a transconductance g_m=17 mS and a current cut-off voltage of over 3 V. In the FET-LD, the drain current is measured against the voltage across the series combination of the laser and the FET. The transconductance is estimated at about 13 mS for V_g=0 V and V_d=5 V. The FET-LD current cut-off condition is a little different from that of the PIN-FET, because the bottom of the gate column neighboring on the laser lies in the n-InGaAs layer, and then the undepleted region formed under the gate column produces the uncontrollable current. This is due to the extraordinary edge growth of InGaAs epitaxial layer in the vicinity of the SiN mask.

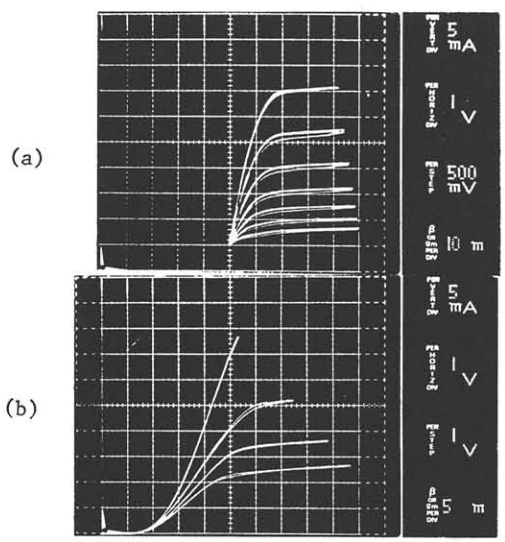

Fig. 4 Static drain-source current variations vs drain voltage.
(a): PIN-FET
(b): FET-LD

Therefore, the unuseful drain current could be reduced by keeping the FET further away from the laser and forming the gate column bottom in a SI-InP substrate.

In Fig. 5, FET gain characteristics (h_{21}) vs frequency are shown. The gate voltage and drain bias voltage were kept at -0.2 V and 3 V, respectively. Open circles indicate the PIN-FET gain characteristics and solid circles correspond to that of a FET in the FET-LD. The f_T of the PIN-FET is about 1.8 GHz, and that of the FET in the FET-LD was 3.5 GHz. For this difference in f_T, the PIN capacitance, which increases the effective gate source capacitance, is responsible.

The light output vs current characteristics of the laser diode is shown in Fig. 6. The threshold current of 20-30 mA was typically obtained. We tested the lasing characteristics of the BH wafer, prior to the InGaAs epitaxial growth. The above threshold current level was almost the same sa that obtained in the test, which indicate that additional InGaAs epitaxial growth, Be-implantation and subsequent flash annealing produced no increase in the laser threshold current.

SUMMARY

A monolithically integrated PIN-FET-LD in the InP system was fabricated using the p-column gate FET and the buried structure laser diode emitting in the 1.3 μm wavelength region. Epitaxial wafers were grown by LPE on a SI-InP substrate. The selectively grown InGaAs layer with carrier density of $1\text{-}2\times10^{16}$ cm^{-3} could be reproduced on the SI-InP surface containing the BH/DH layers covered with the SiN mask. The transconductance and f_T were measured to be about 17 mS and 3.5 GHz, respectively. Typical laser threshold current is about 25 mA and no threshold current increase owing to the additional InGaAs epitaxial growth, Be-implantation and subsequent flash annealing was observed.

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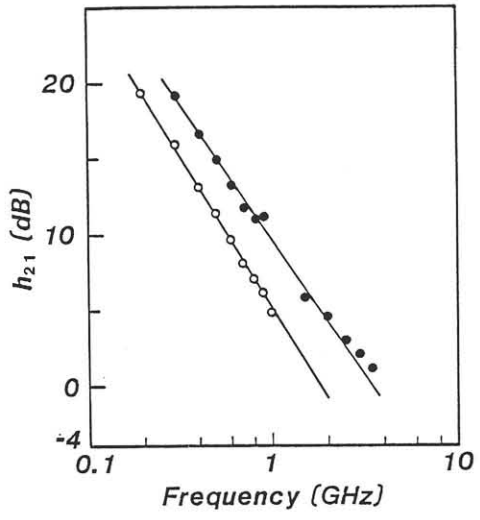

Fig. 5 Dynamic gain characteristics of the FETs incorporated in a PIN-FET(indicated by open circles) and a FET-LD(by solid circles).

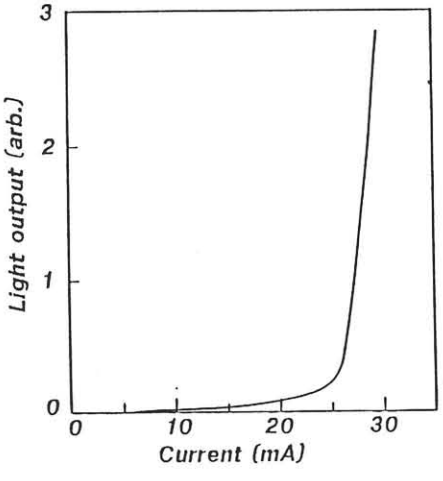

Fig. 6 Light output vs current characteristics of the laser in the PIN-FET-LD.