Reduction of the High Resistive Layer at the Interrupted-Interface of GaAs Grown by MBE

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Desorption of Ga atoms from GaAs films at a high substrate temperature has been utilized as etch-back method for the reduction of high-resistive layers formed around growth-interrupted interface in Si doped GaAs. The mechanism of the reduction of the high resistive layer was studied by a C-V carrier profiling technique, secondary ion mass spectrometry and deep level transient spectroscopy, and clarified as being due to compensation by Si atoms accumulated on the GaAs surface during the thermal etching procedure. The origin of the high-resistive layer was related to the density of Si atoms in air exposed surface.

I Introduction

In molecular beam epitaxy (MBE) of GaAs, it is known that a high-resistive layer is formed around the interface where growth is interrupted. The presence of such an interfacial layer obstructs the realization of novel devices which require the process of growth-interruption exposed to air.

Recently, several methods such as As passivation^{1,2)} or InAs passivation³⁾ have been proposed to suppress these layers, but there are still some problems in the application of these methods for device fabrication.

In order to reduce the high-resistive layer, we employed thermal etching in a growth chamber. GaAs films were etched thermally when the substrate temperature was kept above 650° C with As₄ flux⁴⁾.

In this paper, the effects of this thermal etching on the high-resistive layer and a possible origin of the interfacial layer are reported. To study such an interfacial layer, we employed three methods ; a C-V profiling technique, secondary ion mass spectrometry (SIMS), and deep level transient spectroscopy (DLTS).

II Experimental

We used an MBE 830 (ANELVA) system with an analysis and a load-lock chamber throughout this experiment. Si-doped (100) GaAs was used as a substate for epitaxial growth. The substrate was pretreated in hot $H_2SO_4:H_2O_2:H_2O$ (5:1:1) for 3 minutes before being mounted onto the substrate-holder block with In. Then, the samples were placed in the load-lock chamber and transferred to the growth chamber. GaAs was grown at a rate of 1 μ m/h at substrate temperature T $_{\rm S}$ 580°C with an As₄ pressure producing As-stabilized conditions.

In order to measure the thermal etch rate, samples which consist of a 500 nm thick GaAs layer followed by a 100 nm thick layer of Al_yGa_{1-y}As (x=0.5) and a 10 nm thick cap layer were grown on the substrate. After growth, a half area of the sample was chemically step-etched until a GaAs layer appeared. By using this sample, we were able to measure the thermally etched depth for the GaAs layer from the difference in step-depth change between GaAs and $A1_xGa_{1-x}As$ after thermal etching, because the $Al_xGa_{1-x}As$ layer plays the role of a nask for thermal etching.⁴⁾ The thermal etching was carried out in the growth chamber at a substrate temperature between 680°C and 720°C. The depth of the etching was measured by an interference microscope.

To study the effect of thermal etching on carrier profiles, Si doped samples were grown. The doping levels were 1 - 3 x 10^{16} /cm³ for C-V measurement and 1 x 10^{17} /cm³ for SIMS, For DLTS measurement, 450 nm n-type layer was grown on an air-exposed n-surface followed by p⁺-layer growth

for hole injection. The doping level of the n-region was $3 \times 10^{16}/\text{cm}^3$.

For the carrier profile of the interrupted layer in p-type GaAs, a p-GaAs layer was grown with Be-doping to about 2 x $10^{16}/\text{cm}^3$ on n⁺-GaAs.

III Results and Discussion

The substrate temperature dependence on the thermally etched depth as a function of the etching time is shown in Fig. 1. The As₄ flux was kept constant during the thermal etching. Etching rates greatly increased with rising substrate temperature, and were 3 nm/min at 680°C, 7 nm/min at 700°C and 16 nm/min at 720°C.

Figure 2 shows carrier profiles after interruption, with treatment as follows : A) thermal etching without exposure to air, B) exposure to air and regrowth without thermal etching, and C) thermal etching after exposure to air and regrowth. The carrier peak in sample A indicates the accumulation of Si atoms at the interface. The amount of accumulated Si atoms is about 1.2 x $10^{12}/cm^2$. This value corresponds to the integration of Si distributed in the approximately 600 nm thick etched layer. The accumulation of Si was confirmed through SIMS measurement. Figure 3 shows the Si profile after thermal etching and re-The doping level of this sample was 1 \boldsymbol{x} growth. $10^{17}/cm^3$. Sample B in Fig. 2 which was exposed



Fig.l Thermally etched depth of GaAs films as a function of etching time at three substrate temperatures. As flux was kept constant.



Depth from Surface (µm)

Fig.2 Depth profiles of carrier density after various treatments; (A) thermal etching onlu (closed circles), and (B) exposed to air (open circles), and (C) thermal etching after exposure to air (closed squares.



Depth from Surface (µm)

Fig. 3 Depth profile of Si atoms in GaAs film with thermally etched interface by Sims measurement.

to air shows a large amount of carrier depletion about 5.7 x $10^{11}/\text{cm}^2$. On the other hand, in sample C, which was thermally etched after exposed to air, the high-resistive layer was greatly reduced. If Si atoms which accumulate at the interface become donors, these donors should compensate for the depletion centers and thus prevent the formation of such a high-resistive layer. In the case of thermal etching, roughly half of the





accumulated Si may compensate the carrier depletion. However, for layer doping, the situation is very different. In a n-GaAs with background doping level of $1.5 \times 10^{16}/\text{cm}^3$, layer doping of 2 $\times 10^{17}/\text{cm}^3$ on both sides (each of which are 36 nm in thickness) of the interrupted interface could not compensate the carrier depletion. There was still the carrier depletion of 2.8 $\times 10^{11}/\text{cm}^2$. The increase in the number of carriers at the interfacial layer should amount to 1.4 $\times 10^{12}/\text{cm}^2$, if the layer doped Si had been activated.

Therefore, the total amount of carrier depletion is $1.68 \times 10^{12}/\text{cm}^2$. This large amount of carrier

depletion will be discussed later.

In order to investigate the origin of the highresistive layer, DLTS measurement was performed to detect deep trap levels. As shown in Fig. 4, several electron(EB7) and hole(HL3) trap levels were detected in the high-resistive layer of the $p^{+}n$ junction which has a similar carrier profile to that of sample B in Fig. 2. The HL3 peak(E_c +0.59eV) is probably due to Fe⁵), and the EB7 peak (Ec +0.30eV) is observed commonly in MBE grown GaAs.⁶) However, the total concentration of these trap levels was on the order of $10^{10}/cm^2$. Thus we can not consider these trap levels as the origin of the high-resistive layer.

If the formation of the depletion layer is due to carbon impurities acting as acceptors, then an increase in carriers at the interface can be expected in p-type GaAs. However, carrier depletion was observed in the vicinity of the interface, as shown in Fig. 5. Therefore, it is thought that the origin of the depletion layer cannot be attributed only to the carbon impurities acting as acceptors. Our experimental results of the carrier profile in the vicinity of the p-GaAs interface agree approximately with those reported by D.L. Miller et.al.²

Up to the present, it has been reported $^{1,2,7)}$ that in GaAs doped with Si to 2 x $10^{16}/\text{cm}^3$, the amount of carrier depletion around an interface



Fig. 5 Carrier density profile of Be doped GaAs with exposure to air.



Fig. 6 Carrier density profile of Sidoped (1.2 x $10^{17}/cm^3$) GaAs with exposure to air.



Fig.7 Amount of carrier depletion around the interface with exposure to air vs. carrier density.

which has been exposed to air is $2 - 6 \times 10^{11}/\text{cm}^2$. This indicates that there are large fluctations depending on the condition under which exposure to air took place. The carrier profile around the interface of GaAs doped with Si to $1.2 \times 10^{17}/\text{cm}^3$ is shown in Fig. 6. In this figure, the amount of carrier depletion in the vicinity of the air-exposed interface is $1.5 \times 10^{12}/\text{cm}^2$, which is approximately three times as large as the depletion for doping levels of about 2.0 x $10^{16}/\text{cm}^3$.

Figure 7 shows the change in the amount of carrier depletion at the interface vs. Si doping levels. From this figure, it is clear that the amount of carrier depletion is directly related to the density of Si atoms. These results indicate that layer doping may not be effective. Thus the origin of the high-resistive layer may be attributed to the existence of contaminants such as carbon or oxigen and/or of defects which interact with Si atoms.

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