# Growth of Single Domain GaAs on Si(100) by Molecular Beam Epitaxy

Seiji Nishi, Masahiro Akiyama and Katsuzo Kaminishi

Research Laboratory, Oki Electric Industry Co., Ltd. 550-5 Higashiasakawa, Hachioji, Tokyo 193

Single domain GaAs layers were grown on Si(100) substrates by MBE. Raman spectra were measured on these layers and only LO phonon peak was observed. Etch pit density of epitaxial layers were about 2000cm<sup>-2</sup> and TEM micrograph showed the high dislocation density near the hetero interface decreased with the thickness of epitaxial layer. These measurements confirmed good crystalline GaAs layers were grown on Si(100) substrates.

# Introduction

Heteroepitaxial growth of GaAs on Si substrate has been interested. The Si substrate has many merits compared with GaAs substrate, for example large area, low cost, high thermal conductivity, easy handling, etc.. Several works have been reported on the growth of GaAs on Si by  $MBE^{1)\sim5}$  and  $MOCVD^{6}$ , and single domain GaAs layers were successfully grown on Si substrate using the GaAs buffer layer grown at low temperatures.<sup>5),6)</sup> In this study, single domain GaAs layers were grown on Si(100) substrate by MBE. Raman spectra were measured on these layers. Defects in the epitaxial layers were studied by chemical etching and TEM observation.

# Crystal Growth

The MBE system used in this study was ANELVA 830S. The growth rate was about  $0.8\mu$ m/h. The substrate temperatures were monitored by the thermocouple behind a Mo sample holder. The RHEED was used to monitor the surface condition during the growth. After the removal of the oxide layer by HF, Si(100) wafer was fixed to the Mo sample holder by In solder, followed by loading into the MBE system. By these procedure, Si surfaces were covered with thin amorphous oxides. These oxides were removed only by raising the substrate temperatures to about 850°C. On the



Fig.1 Time chart of substrate temperatures used in this experiments to grow GaAs on Si substrate by MBE.



(a)



(b)

Fig.2 RHEED patterns after the growth of  $1.5\mu$ m GaAs with the buffer layer grown at 300°C. (a) [011] azimuth. (b)[011] azimuth.

thermally cleaned Si substrate, 1.5 $\mu$ m GaAs layers were grown after the 100Å GaAs buffer layers grown at four different temperatures(Tb). The time chart of the substrate temperature is shown in Fig.1. In each case, before the growth of the top GaAs at 600°C on the buffer layer, RHEED patterns were spotty, they changed to be streak after 1000Å GaAs were grown. The clear 2x4 reconstructed patterns observed after the growth of 1.5µm GaAs are shown in Fig.2. The same reconstructed patterns were observed when the electron beam was scanned across the wafer, indicating the single domain GaAs layers were grown on the whole area of a 2-inch Si substrate. The intensity of 2x4 patterns at the end of the growth were a little weak when the substrate temperatures of the buffer layer were high. Mirror surface GaAs layers were grown with the buffer layers grown at 150°C and 300°C, but at 400°C and 600°C the surfaces were milky. These growth conditions were reported previously.<sup>5)</sup> It was shown by some workers<sup>1),3),4)</sup> that an initial arsenic overpressure was necessary for epitaxial growth. We grew GaAs with a buffer layer grown at 150°C without As beam before 1-2 monolayer Ga were deposited (As cell temperature was kept at R.T.). RHEED after 1-2 monolayer Ga deposition showed 2x2 streak pattern, but after As beam exposure, the RHEED pattern changed to be from streak to spotty, these changes of pattern were not observed when only As beam was exposed before Ga beam exposure. After the growth of GaAs, clear 2x4 RHEED patterns were observed and the surface morphology of GaAs layer was good, indicating a As primer layer is not always necessary to grow a single domain GaAs layer on a Si substrate.

## Raman measurement

The surface morphology of GaAs layers with buffer layer grown at 150 °C and 600 °C are shown in Fig.3. The photographs show that the surfaces are a little wavy in a common direction in the single domain region, and on the layer with the buffer layer grown at 600 °C, there are many surface defects. Raman measurements were performed on these layers(Fig.4). In the Raman spectra from the GaAs layer with the buffer layer grown at 150 °C, only L0 phonon peak was observed whose half width was comparable to that of the bulk GaAs. On the GaAs layer with the buffer layer grown at 600 °C, micro Raman measurements from defect region and flat region were performed(Fig.4(b),(c)). The large half widths of these spectra were caused by the large light intensity in micro Raman measurements. In the Raman spectra from the flat



10 µm — (ь)

(a)

Fig.3 Nomarski microphotographs of  $1.5\mu$ m GaAs layers on Si(100). The buffer GaAs layers were grown at (a)150 °C and (b)600 °C.



Fig.4 Raman spectra of  $1.5\mu$ m GaAs films on Si(100). (a)Macro Raman spectrum. The buffer layer was grown at 150°C. (b)(c)Micro Raman spectra. The buffer layer was grown at  $600^{9}$ C. (b)On the flat region. (c)On the defect region. region, only LO phonon peak was observed, but in that from defect region, both of LO and TO phonon peaks were observed.

From the Raman measurements, the good GaAs layers were grown in the single domain region, but when the growth temperature of a buffer layer was high, many defects were observed on the surface and near these defects TO phonon peak was observed, indicationg the other surface component from (100) was contained. We expect that, when the growth temperature of buffer layer is high, the growth with the other surface starts easily on a Si surface.

## Defects in the epitaxial layer

On the almost all area of a 2-inch Si(100) substrate, GaAs layer was grown with a single domain, and at the half of the near edge of the wafer, domain boundary was observed. We expect that Si(100) surfaces are a little tilted and the direction of the tilt suppresses the antiphase domain formation. On the GaAs layers with the buffer layer grown at 150°C, etch pit density was measured. Etching was carried out by molten KOH at 400°C for about 10sec. Near the domain boundary mentioned above, many etch pits were observed(Fig.5(a)). But apart from the domain boundary to about 0.2mm, etch pit density decreased drastically. On the single domain region, etch pit density was about 2000cm<sup>-2</sup> and most of these pits were caused by oval defects(Fig.5(b)).

We performed the cross-sectional TEM observation on the GaAs layer with the buffer layer grown at 150°C(Fig.6). Near the interface of GaAs and Si, many dislocations are observed in TEM micrograph, which may come from the 4% difference of lattice constants between GaAs and Si. These dislocation density decreases with the thickness of GaAs layer. The low dislocation density at the surface of  $1.5_{\mu}m$  GaAs, even though the high dislocation density at the interface, is consistent with the low etch pit density.

The dislocation density near the surface of  $1.5_{\mu}m$  GaAs layer on Si is found to be sufficiently low (~2000cm<sup>-2</sup>) to fabricate devices and may be reduced if the density of oval defects could be reduced.



10µm ——

(a)

Fig.5 Nomarski microphotographs of etched surfaces by molten KOH. The buffer layer was grown at 150°C. (a)Single domain region. (b)Near the domain boundary.

(b)



Fig.6 Cross-sectional TEM micrograph of  $1.5\mu m$  thick GaAs layer on Si(100) substrate.

Summary

Single domain GaAs layers were grown on Si(100) substrates by MBE. The buffer layer at low substrate temperature was effective to grow a good crystalline layer, which was confirmed by the Raman spectra measurement. From the cross-sectional TEM measurements, although the dislocation density near the hetero interface was high, it was observed to decrease with the epitaxial layer thickness. The etch pit density of the  $1.5_{\mu}m$  thick epitaxial layer was low enough (~2000cm^{-2}) to fabricate devices on the GaAs layer.

### Acknowledgement

This work was performed under the management of the R & D Association for Future Electron Device as a part of the R & D Project of Basic Technology for Future Industries sponsored by the Agency of Industrial Science and Technology, MITI.

## References

- 1) W.I.Wang, Appl.Phys.Lett.44,1149(1984).
- 2) G.M.Metze et.al., Appl. Phys.Lett. 45, 1107(1984).
- 3) W.T.Masselink et.al., Appl. Phys.lett.45,1309 (1984).
- 4) A.Christon et.al., Electron.Lett.21,406(1985).
- 5) S.Nishi et.al., Jpn.J.Appl.Phys.24, L391(1985).
- 6) M.Akiyama et.al., Jpn.J.Appl.Phys.23, L919(1984).