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Recent Advances in High Speed Bipolar LSI Technology

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To manufacture high speed LSIs, advanced structure and processes, such as scaled oxide isolations, SST, SICOS, OXIS Ⅲ, IOPⅡ, have been studied. In this paper, recent advances in high speed bipolar LSI technology will be described. Future prospects are also considered.

§1. Introduction

There is greater demand for higher system speed because of manufacturing large computers, large-capacity optical fiber transmission systems, high-speed switching systems, and electric measuring instruments. These systems applications require high-speed integrated circuits with less than 100 ps/gate. To manufacture higher speed ICs, advanced structure and processes of silicon bipolar ICs have been studied.

Using 1.25μm lithography, 2000～5000-gate masterslices with 220～350 ps/gate basic gate delay time and a 4 Kb ECL RAM(1)with an access time of 2.3ns have already been developed.

Generally, reduction of parasitic elements, such as collector-base junction capacitance and base resistance, and higher cut-off frequency are most effective for increasing speed in bipolar ICs. In order to decrease these parasitic elements, advanced transistor structure and processes, such as SST(2)(3)(4), SICOS(5), have been studied.

In this presentation, resent advances in high speed bipolar LSI technology will be described. Future prospects are also considered.

§2. Advanced Structures, Processes and its Application

2.1 Scaled Oxide-Isolation Technology

A 64 Kb bipolar SRAM(6)with a cell size of 190μm^2 and 2μm features has been fabricated. Silicided polysilicon has been used to interconnect crosscoupled transistors, polysilicon resistors as load devices, and lateral polysilicon diodes for bit-line coupling devices. The access time of the RAM is 15 ns with power dissipation of 900mw.

A 150ps 9K-gate ECL masterslice(7)has been fabricated using OXIS III. A cross section of a transistor using OXIS III is shown in Fig. 1. One of its features is a self-aligned emitter-base structure with polysilicon emitter and base. The propagation delay time of an internal OR-NOR-CM gate is 200ps/gate, with a speed-power product of 1.2pJ/gate. To make optimum use of the 9000 gates, a total of 256 logic and 64 power supply pins are provided. Typical power dissipation of the devices is 20W.

2.2 Side Wall Base Contact Structure; SICOS(5)

The transistor structure is shown in Fig. 2. Base areas, emitter areas, base contact, base electrode and oxide isolation areas are defined by only one photomask pattern. Parasitic elements, such as base resistance, collector-base junction capacitance, and isolation capacitance are reduced. The NPN transistor has a symmetrical structure. The downward and upward cut-off frequencies are 14 GHz and 4GHz, respectively.

A 6GHz ECL frequency divider(8)with

46mW/stage power dissipation and a 580 MHz I^2L frequency divider with 9 mW/stage power dissipation, have been realized using SICOS.

2.3 Trench Isolation Technology

Cross sections of IOP-II are shown in Fig. 3. Using IOP-II, it is possible to eliminate the parasitic isolation capacitance in addition to the scaling effect. A 64Kw x 1b ECL RAM(9) with two array redundancy has been fabricated in IOP-II and 1.2 μm lithography. The address access time of the RAM is 10 ns with power dissipation of 1.3W.

2.4 Self-aligned Technology with non-LOCOS Oxide Isolation Using Selective Growth of Poly-and-Single-Crystalline Silicon(10).

A transistor structure using this technology is shown in Fig. 4. The emitter region, formed in the recessed single-crystalline silicon region, is self-aligned to the polysilicon base contact and also the isolation oxide area. One micron or submicron emitter width is easily obtained without fine lithography. Propagation delay times of basic low-level CML are 190 ps/gate at 0.22 mW/gate and 83 ps/gate at 1.0 mW/gate, respectively.

2.5 Super Self-aligned process Technology; SST

(1) Structure

In SST, only one mask is needed to produce the emitter and base regions, including the submicron width base electrode, base and emitter contacts. Figure 5 illustrates the structure of an integrated npn transistor using the recently developed SST-1A compared with that using conventional oxide isolation. The transister has a 0.35 μm-wide emitter and 1.57 μm-wide base region.

(2) Basic Gate Performance.

Propagation delay times were measured for NTL and LCML 51-stage ring oscillators. For the NTL, using transistor with 0.35 x 10 μm emitters, 30 ps/gate was achieved at 1.48 mW/gate. For the LCML, using transistors with 0.35 x 5 μm^2 emitters, the propagation delay time of 50 ps/gate was achieved at 1.46 mW/gate.

(3) 4~5.7 Gbit/s Logic Family

A Si bipolar 4~5.7 bit/s logic family with 50 ohm load driving capability has been developed for high-speed digital systems and optical fiber transmisson systems. The family(11)consists of several kinds of ECL logic (e.g. OR/NOR, D-F/F), and special logic for transmisson systems (e.g.decision circuit). A typical wave form for the 1/8 divider using SST transistor with cut-off frequency f_T =17.1 GHz (Vce=3V), at 9.1 GHz, is shown in Fig. 6.

A 4:1 time-division MSI multiplexer and demultiplexer(12) are fabricated using SST. The maximum operation speed of the multiplexer is 5.02 GHz with 576 mW power dissipation. The system, which is composed of a multiplexer and a demultiplexer, operates up to 4.80 GHz. The fastest multiplexer to date is a GaAs circuit operating at 5 Gbit/s. The maximum operation speed of this new multiplexer is equal to the top speed achieved with GaAs technology; moreover, power dissipation is considerately lower than GaAs ICs.

(4) Very High Speed RAM

An 1Kb ECL RAM with typical address access time of 0.85ns(13) has been obtained using SST and novel circuit technology. The access time of the RAM shows in Fig. 7 compared with those of high speed RAMs reported to date. The RAM using SST is the first RAM with access time of less than 1 ns at room temperature.

(5) Very High Speed Logic LSI.

An ultra-high speed 2,500 gate bipolar masterslice LSI(14) with a fundamental gate delay (LCML NOR with an emitter-follower) of less than 80 ps/gate was fabricated using SST with 1 μm lithography. The power dissipation was 2.61 mW/gate resulting in 0.2 pJ/gate. The experimental results are summarized in Table 1. The propagation delay time for a one milimeter interconnection almost becomes the same order as a fundamental gate delay time. The decrease in interconnection delay time is one of most important problems in developing

a high speed logic LSI.

The feasibility of using a macrocell array LSI was established through the test fabrication and measurement of a 16×16 bit parallel multiplier. The resulting multiplication time was as fast as 7.5 ns with a power dissipation of 2.1 W. The 16x16 bit multiplier using SST is faster than the fully custom-designed 10.5 ns GsAs 16x16 bit multiplier. When a 16×16 bit multiplier with CLA is fabricated on this masterslice, the multiplication time will be about 6ns as shown Fig. 8.

§ 3. Future of Bipolar LSI.

To estimate the performance of future bipolar LSIs, devices consisting of extremely small transistors with 0.2 μm emitter widths were analyzed through a two-dimensional device simulator. The transistor cut-off frequency was about 40 GHz. The cut-off frequency of Si transistor with a hetero structure emitter, such as an amorphous SiC:H(15) emitter, is expected to be more than 40 GHz.

The SST-1A, with submicron rule lithography, can realize high speed NTL circuits functioning at less than 10 ps/gate(F/I=F/O=1) by using a transistor with more than 25 GHz. A 1 Kb RAM with access time of 0.2～0.4 and 2～3KG masterslice with basic gate delay time of less than 50 ps/gate is expected in the near future.

§ 4. Summary

New structures and processes of Bipolar LSI were mentioned above. It is believed that sub-500 ps bipolar RAMs and sub-50 ps/gate 2～3KG bipolar logic LSI will be realized by both self-aligned process technology (such as SST) and submicron rule lithography.

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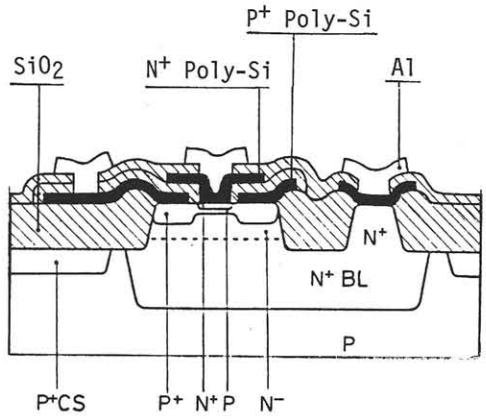

Fig.1 Transistor structure using OXIS-III (Ref.7)

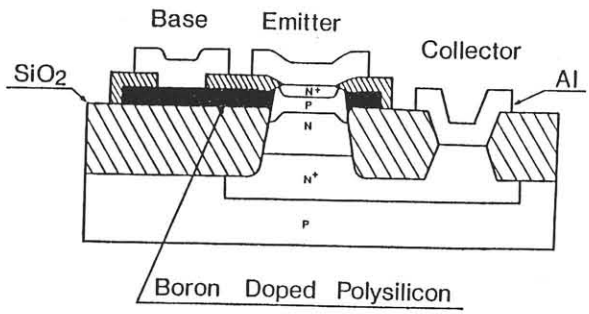

Fig.2 SICOS transistor structure (Ref.5)

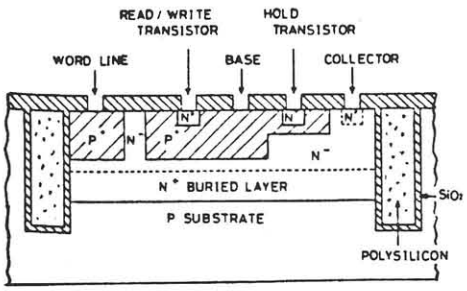

Fig.3 Cross section of a memory cell using IOP-II (Ref.9)

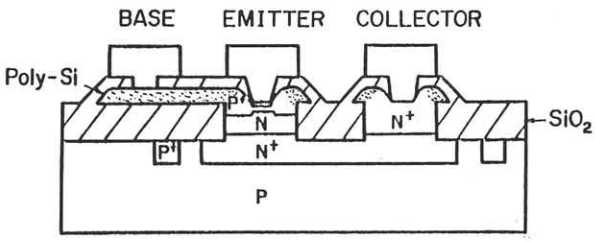

Fig.4 Oxide isolation using selective growth of poly- and single-crystalline silicon (Ref.10)

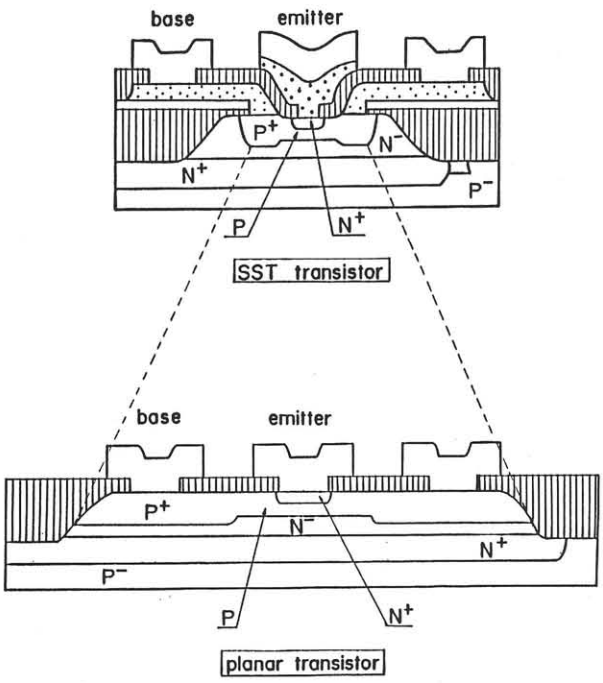

Fig.5 Transistor structure using SST

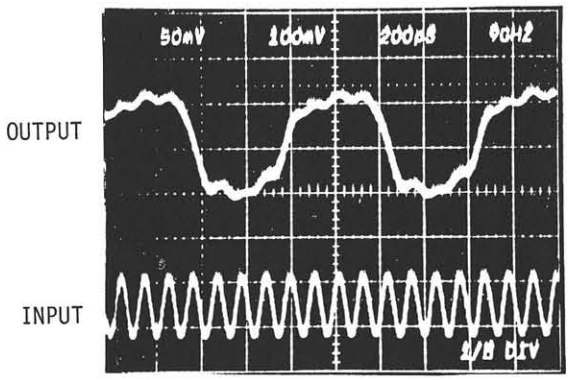

Fig.6 A typical waveform for the 1/8 divider

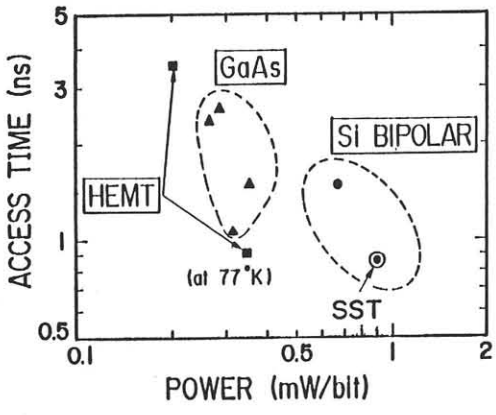

Fig.7 Access time of high speed RAMs

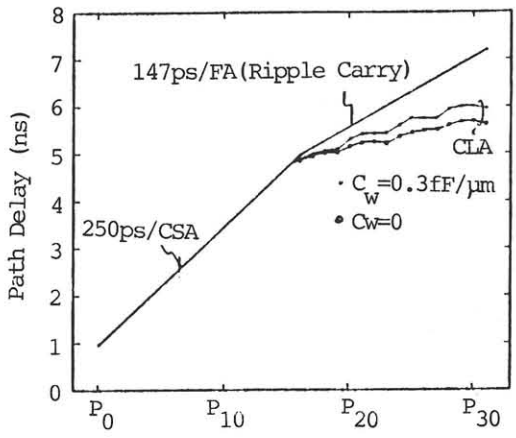

Fig.8 Multiplication time of a 16x16 bit multiplier with CLA

Table 1 Experimental results

LCML gate delay, FI=FO=1	78 ps/gate
Fan-in delay	14 ps/FI
Fan-Out delay, I_{EF}=0.27 mA	19 ps/FO
Metal delay, I_{EF}=0.27 mA	64 ps/mm
I_{EF}=0.41 mA	44 ps/mm