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A 2.1-GHz 56-mW Two-Modulus Prescaler IC Using Salicide Base Contact Technology

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This paper describes a new process technology, called SCOT (Salicide base COntact Technology) for realizing high performance bipolar ICs. The main feature of this process is a base contact formation for reduction of the base resistance and capacitance which are significant transistor characteristics as a result of ECL gate speed analysis. The base contact in the SCOT process is produced by the silicidation of the self-aligning opened both the P^+-polysilicon and base region. 1/128, 1/129 two-modulus bipolar ECL prescaler ICs with the use of the SCOT process have been improved to a high operation of 2.1 GHz at 56-mW power dissipation or a low power dissipation of 30 mW in 1.4-GHz operation.

1. Introduction

For mobile radio systems and satellite communication receivers, prescaler ICs have been required to operate at a high frequency, at about the GHz band, and also with low power dissipation. The 1.6-GHz 63-mW dual modulus Si prescaler IC (1), and 1.1-GHz 50-mW GaAs prescaler IC (2) have been reported as suitable to this requirement. The two-modulus prescaler ICs which are used mainly in digital tuning systems are needed for operation at about 1 GHz, in spite of the fact that each channel has a very narrow band width. The first-stage flip-flops which take the greatest part of the IC power dissipation, dissipate about three times more than that of the fixed prescaler. Accordingly, it is very important to set up an optimum transistor for the high operating prescaler IC at the low power dissipation.

The optimum transistor design for the high performance devices were estimated by using circuit simulation. A new proposed transistor was realized with the base contact of a Self-Aligned Silicide (Salicide) structure which was made by silicidation of polysilicon and silicon surface simultaneously in the same way as MOS technology (3). By the SCOT process, the feature of the transistor was improved and the high performance of two-modulus prescalers were obtained.

2. Gate Speed Simulation

The principal transistor parameters limiting gate speed have been studied by computer-aided simulation (4). The propagation delay time tpd of the ECL inverter was calculated concerning the transistor parameters so that the collector-base capacitance C_{TC}, forward base transit time τ_F, base series resistance r_B and so on by used of circuit simulation SPICE-II (5).

The parameters of the conventional bipolar transistor ISAC (6) whose emitter size was $2 \times 4\ \mu m^2$, were used as the initial value x_0. The sequence of simulations tpd(x) was performed in the varied parameters individually. As a result, the contribution of parameters limiting the gate speed were investigated. Fig. 1 shows the sensitive specific of tpd for gate current Ig. The sensitive specific S was defined as follows;

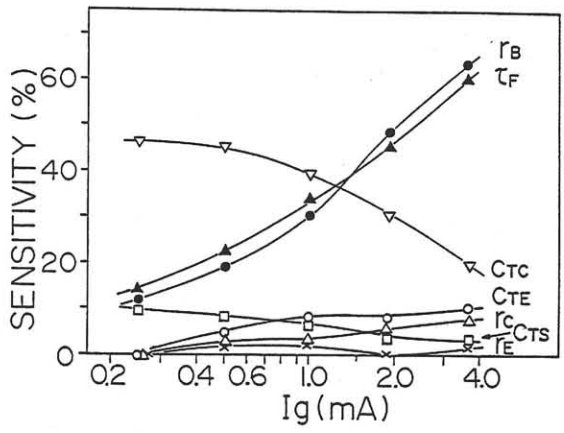

Fig.1 Sensitive specific of gate speed versus gate current.

$$S = \frac{t_{pd}(X) - t_{pd}(X_0)}{t_{pd}(X_0)} \Big/ \frac{X - X_0}{X_0}$$

where x was the each transistor parameter. The gate current was the sum of switching and emitter follower current. It is clear in Fig. 1 that the C_{TC}, τ_F and r_B are mainly effective transistor characteristics for high-speed performance. We should consider such a transistor design because the C_{TC} was reduced at low current operation, under 0.3 mA of gate current, and because the r_B and τ_F were reduced at over 4 mA operation. If the three factors are reduced at the same time, a high-speed transistor is realized at a wide current range and also the additive effects of the three factors are expected at about 1 mA of gate current.

3. Fabrication Process and Transistor Design

Fig. 2(A) illustrates the top view of the npn transistor fabricated by the SCOT process (SCOT transistor), and Fig. 3 shows the key step in the processing sequence of the SCOT transistor. The isolation of the SCOT transistor was comprised of the full-recessed oxidation for the transistor isolation and the semi-recessed oxidation surrounded on the base area. The cross-section of isolation oxide was the stairs structure shown in Fig. 3(A). The first polysilicon layer was formed on the base edge extended over the isolation oxide in order to connect the base Al electrode and silicide contact. The resistance was fabricated at the same time with the P^+-polysilicon layer. After the base region was made by the boron implantation, the emitter window was opened and the second polysilicon layer deposited over all surfaces was implanted with a heavy dose of arsenic ions, as shown in Fig.3 (B). The emitter region was produced by the diffusion from the N^+-polysilicon layer and that, except the emitter polysilicon electrode, was etched off by the RIE. The SiO_2 layer at the base contact and the P^+-polysilicon layer were etched away by using the photo-resist mask of emitter polysilicon etching, as shown in Fig. 3(C). The thick oxide was selectively grown over the high arsenic doped emitter polysilicon in wet oxidation at 820℃ by exploiting the effect of concentration dependent oxidation (7). Therefore, the oxide surrounding the emitter polysilicon remained after removal of the thin oxide on the base contact and P^+-polysilicon, and separated the base contact from the emitter polysilicon. The Pt-silicide was formed both on the epitaxial surface of the base contact and the P^+-polysilicon surface, as shown in Fig.3 (D). The base electrode was fabricated with both the silicide of the self-aligning opened base contact and the polycide, and then this could be called a salicide (self-aligned silicide) base

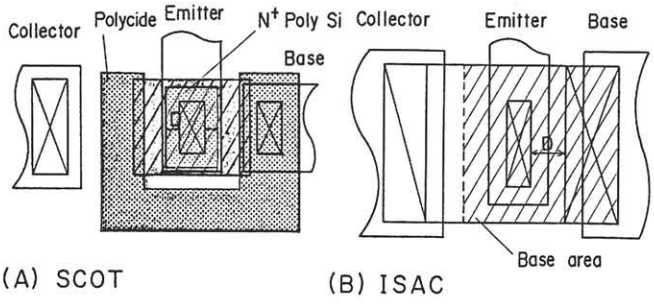

Fig.2 Schematic layout of a SCOT transistor and ISAC transistor.

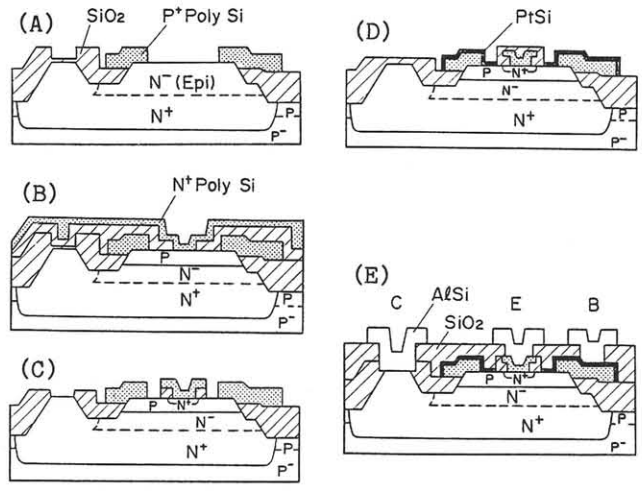

Fig.3 Fabrication procedure of SCOT process.

Table 1 Characteristics of npn transistor with the SCOT process

Epitaxial thickness	1.6 μm
Base resistance	1 kΩ/□
Base depth	0.23 μm
Emitter depth	0.1 μm
P^+-Polysilicon resistance	200 , 400 , 650 Ω/□
Polycide resistance	8 Ω/□
Contact size	1.5 x 3.0 μm^2
Aℓ line /space	3.5 μm / 2.0 μm
h_{FE}	80
BV_{CEO}	9 V

contact. Opening the contact windows of the collector and emitter in the N^+-polysilicon and the base in the P^+-polycide and the Al-metallization completed the processing of the SCOT transistor, as shown in Fig. 3(E). The process sequence, the design rule and the DC parameters of the SCOT transistor are detailed in Table 1.

As a result of the gate speed analysis of the transistor characteristics, the important characteristics were the C_{TC}, τ_F (f_T) and r_B for high-speed performance. It was learned by the following comparison with the ISAC transistor, as shown in Fig. 2(B), that the SCOT transistor has realized the optimum transistor design with reduction of those characteristics. The first factor, reduction of r_B in the SCOT transistor, was conducted by decreasing the distance D between the base contact and emitter and by the double-base structure, as shown in Fig. 2. The distance D, in the case of the SCOT transistor, was determined by the salicide base contact structure and was close to 1 μm in a half value of the ISAC one. The base area in the SCOT transistor, for the second factor, reduction of C_{TC}, was decreased to approximately half the time of that in the ISAC one. In order to decrease the active base region, the emitter length can be decreased as the goal to maintain a small r_B. The reduction of the parasitic base region was achieved by the full walled base structure with the stairs oxide isolation and by the salicide base contact structure. The vertical down-scaling, in which the depth of the emitter-base junction was 0.1 μm and the base width was 0.13 μm, produced the higher f_T. A synthesized transistor design for high-speed performance has been obtained with the SCOT transistor.

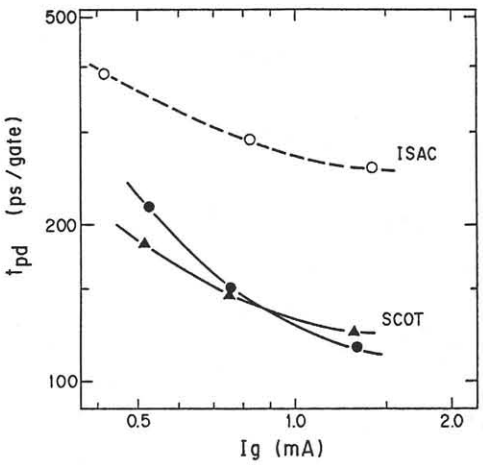

Fig.4 Relations between gate speed and gate current in various ECL ring-oscillators. The tpd's with 1.5μm x 5μm emitter are shown in the solid and open circles, and the solid triangles correspond to 1.5μm x 3μm emitter.

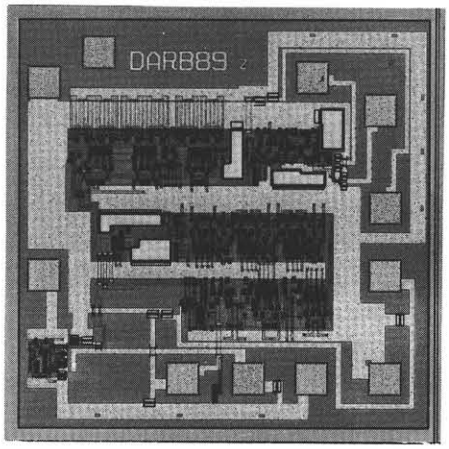

Fig.5 Photograph of a two-modulus prescaler IC. Chip size is 1.56mm x 1.56mm. 1st level metallization of AlSi and cross-overs of polycide are employed.

4. Device Characteristics and Prescaler IC

Table 2 shows the performance of the SCOT transistor by use of the prescaler IC. Compared with the current product with the ISAC process, the C_{TC} and r_B decreased to half value and f_T became twice the value. According to the relationship of the sensitive specific in Fig. 1, each of the three characteristics of the SCOT transistor improved in the ECL gate speed by about 80% respectively. The simulated value tpd(x) of the SCOT circuit became 152 ps by using 267 ps tpd(x_0) of the ISAC circuit and was in good agreement with the measured 140 ps. Moreover, the maximum cutoff frequency obtained was 9.5 GHz at Ic= 6 mA by the SCOT transistor in which the emitter was 1.5 μm x 5 μm x 4 fingers.

Fig. 4 shows the tpd of the ECL gate circuit by using the SCOT process and the ISAC

Table 2 **Comparision of features of newly developed prescaler and current prescaler.**

		New development	Current product
Process technology		SCOT	ISAC
Emitter size		1.5 x 3 μm²	1.5 x 5 μm²
Emitter depth		0.1 μm	0.4 μm
Capacitance	C_{TC}	9 fF	20 fF
Base resistance	r_B	49 Ω	92 Ω
Cutoff frequency	f_T	4.1 GHz	2.2 GHz
Delay time of Ring-osc.		140 ps	267 ps
Max. operating frequency		2.1 GHz	1.1 GHz
Power dissipation		56 mW	125 mW

process. The tpd in the SCOT process on the same emitter size was remarkably fast, especially at the high current range by effect of reducing r_B. The mimimum tpd achieved 116 ps at gate current Ig= 1.3 mA. When the emitter length was decreased from 5 μm to 3 μm in Fig. 4, the tpd became fast in low current because of decreased C_{TC}, and became late in high current because of increased τ_F and r_B. This conception was consistent with the result of the simulation shown in Fig. 1.

A 1/128, 1/129 two-modulus prescaler IC was fabricated with SCOT transistors and polysilicon resistances. A microphotograph of the chip is shown in Fig. 5. A bypass-condenser in order to obtain suitable operation at high frequency was fabricated by oxidation capacitance with the polysilicon. The power supply was 5 V and the voltage swing was 280 mVp-p. Fig. 6 shows the relation between input signal level and the operating frequency. This prescaler operated in a wide range from 400 MHz to 2.1 GHz with 56 mW at the input signal level -4 dBm.

In Fig. 7, the performance of the SCOT prescaler was compared with other products. The SCOT prescaler had four times higher performance than the ISAC prescaler, and operated with half the power dissipation of the reported ones, (1) and (2). Decreasing the power dissipation by means of increasing the polysilicon resistance, we obtained 1.4 GHz with 30 mW and 850 MHz operation with only 19 mW.

5. Conclusion

We have analized the effect of transister parameters on tpd using circuit simulation, and considered the optimum structure. As the excellent structure with reduction of the C_{TC}, τ_F and r_B simultaneously, the SCOT process has been proposed, and the 1/128, 1/129 two-modulus prescaler has achieved 2.1-GHz operation with 56-mW power dissipation. This result is higher performance than obtained by GaAs technology up to date.

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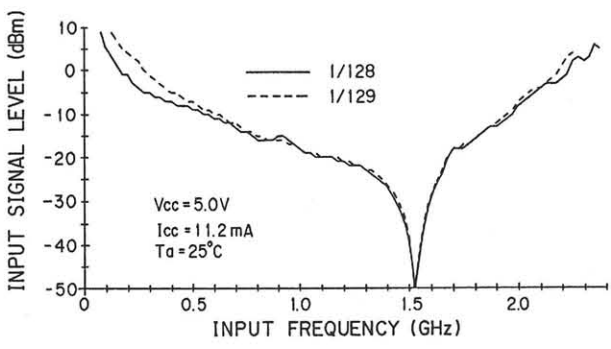

Fig.6 Input signal level versus operating frequency.

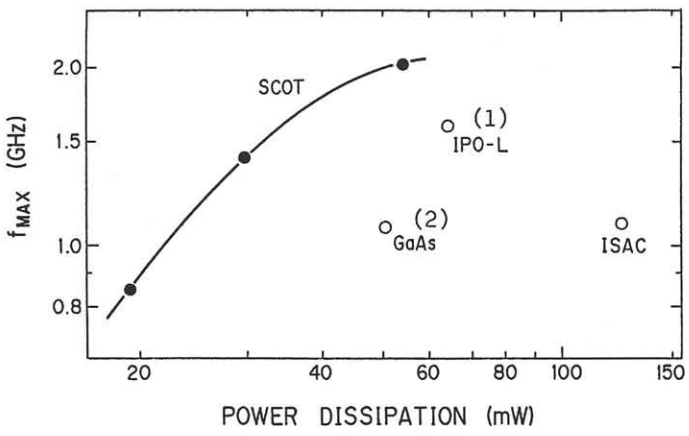

Fig.7 Comparison of maximum operating frequency and power dissipation.