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High Transconductance GaAs MESFETs Fabricated Using Sidewall-Assisted Self-Alignment Technology (SWAT)

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Abstract—A high transconductance (g_m) of 602 mS/mm has been obtained in 0.3 μm-long gate GaAs MESFETs using a combined sidewall-assisted self-alignment technology[1] and WSi_x gate n^+ selective ion implantation technology[2]. The gate orientation effect for the fabricated FET is enhanced by lateral diffusion of implanted n^+ impurities to the channel region. 25-stage ring oscillators with an E/D DCFL configuration were also fabricated using 0.7 μm-long gate FETs. The minimum propagation delay time of 16 ps/gate was observed.

INTRODUCTION

GaAs LSIs are rapidly approaching to practical applications in recent years. To obtain high speed performance from GaAs LSIs, improvement of GaAs MESFET g_m, hence, reduction in the source series resistance (R_S) is inevitable. From this point of view, the authors proposed a GaAs MESFET technology named SWAT (Sidewall-assisted Self-alignment Technology), where the gate and the ohmic contacts are narrowly separated by thin (~0.2 μm) dielectric films formed on both sides of the gate electrode[1]. A 12×12 bit multiplier[3] and a 4 kbit SRAM[4] have demonstrated the feasibility of the technology.

In this work, the selectively ion-implanted contact regions have been newly introduced by adapting a tungsten-silicide (WSi_x) refractory gate to realize a further reduction in the R_S. The n+ implantation effect was studied not only from transconductance viewpoint, but also for the gate orientation effect in the FETs.

DEVICE FABRICATION

The main purpose of this paper is to clear up the effect of n+ contact region in SWAT FETs. For this purpose, three kinds of SWAT FETs, as shown in Fig. 1, were fabricated. Structure (A) is a conventional SWAT FET without n+ layer, which the authors reported before. Structures (B) and (C) are new SWAT FETs having n+ layers outside and inside the SiO_2 sidewall, respectively.

The structure (C) FET fabrication processing

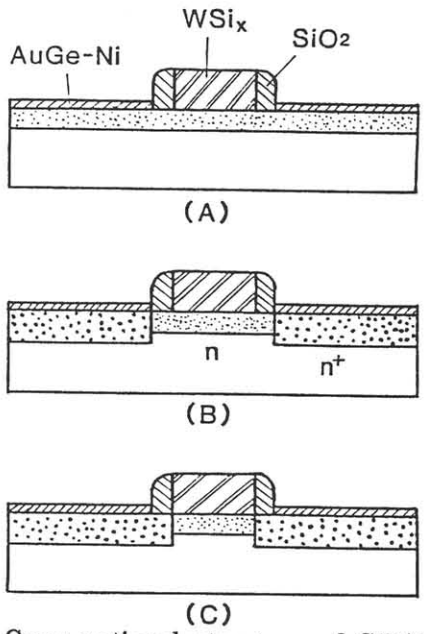

Fig.1. Cross-sectional structure of SWAT FETs investigated in this work

sequence is depicted in Fig.2. In the case of structure (A) devices, no second Si ion implantation is necessary. For structure (B) device fabrication, another SiO_2 sidewall formation was needed before the second ion implantation, where the sidewalls served as a mask for it, together with the gate.

A lightly Cr-doped semi-insulating LEC (100) GaAs wafer was used as a substrate. Selective Si ion implantation provided an n-type channel layer with a 3.2×10^{12} cm^{-2} dose at 30 keV. A 0.5 μm-thick WSi_x film was deposited and the gate electrode was formed by reactive ion etching (RIE). It served as a mask for the second implantation of $1\sim2.5\times10^{13}$ cm^{-2} Si ions at 70 keV for the n+ layer. The implanted n and n+ layers were annealed simultaneously with a Si_3N_4 cap in H_2 atmosphere at 800°C. After the annealing process,

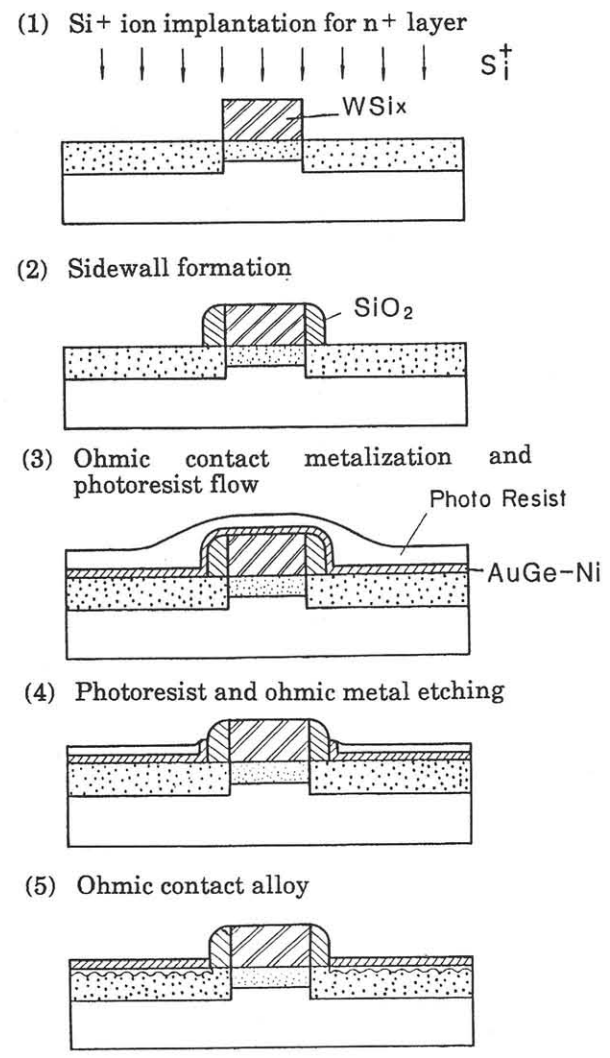

Fig. 2. Device fabrication processing sequence for strucutre (C)

SiO_2 film was deposited. Then, the sidewalls were formed by RIE[1]. After that, the ohmic metal (AuGe-Ni) was deposited over the gate. Then, the metal film on the top of the gate was selectively removed by RIE and Ar ion milling. The separated ohmic metal was spike alloyed in H_2 ambient gas at 420°C.

DEVICE CHARACTERISTICS

At first, a comparison is made concerning the gate length (L_g) dependence of source series resistance threshold voltage (V_{th}) and transconductance (g_m) as shown in Fig. 3. The figure indicates that the V_{th} dependences on L_g for structures (A) and (B) are almost the same. This means that the lateral diffusion of n+ impalnted

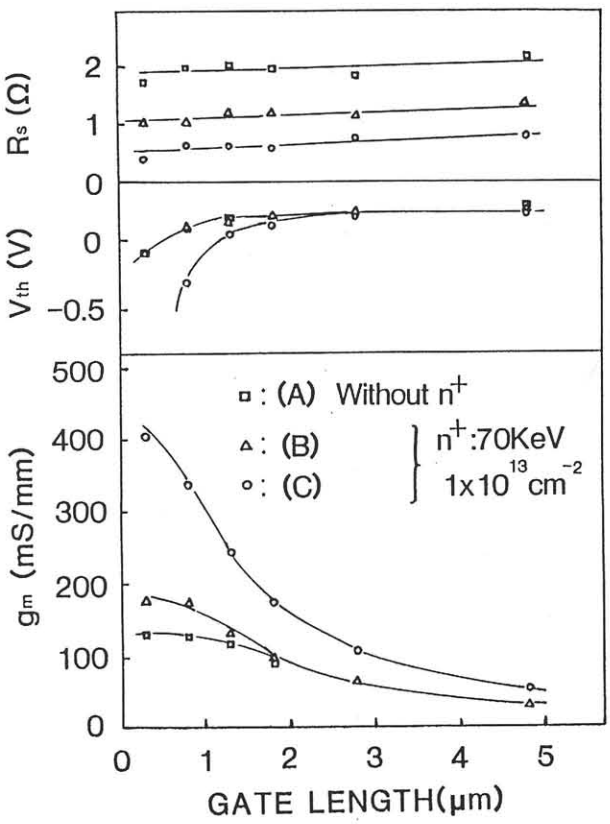

Fig. 3. Gate length dependence of source series resistance (R_S), threshold voltage (V_{th}) and transconductance (g_m) for three SWAT FETs. (n: 30 keV, 3.2×10^{12} cm−2).

impurities has no influence on the channel region beneath the gate electrode in structure (B) because of the existence of the 0.2 μm-thick sidewalls. This has also confirmed the fact that the intrinsic transconductance (g_{mo}) values, calculated from measured g_m and R_S, are completely the same for these device structures ($g_{mo}=160$ mS/mm, for $L_g=1.3$ μm).

On the other hand, in the case of structure (C), where the n+ implantation is introduced adjacent to the gate electrode, a further increase in the g_m value can be expected. The main causes for the g_m improvement are the reduction in R_S beneath the sidewall and the increase in the effective channel carrier density, due to the lateral diffusion of the implanted n+ impurities.

FET parameters for structures (B) and (C) are compared in Table 1. V_{bi} in Table 1 denotes the built-in potential, whose value was assumed as 0.8 V in this work. At $L_g=0.7$ μm, g_{mo} for the structure (C) is 2 times larger than that for structure (B), while $(-V_{th}+V_{bi})$ is 1.5 times larger. By assuming

Table 1 Characteristics comparison between structures (B) and (C) devices.

Device parameters	(B)	(C)
R_s (Ω)	1.1	0.6
g_m (mS/mm)	176	337
g_{mo} (mS/mm)	218	422
$-V_{th}+V_{bi}$ (V)	0.69	1.08

(n: 30 KeV,3.2x10^{12} cm^{-2} ,n^+: 70 KeV,1x10^{13} cm^{-2})

that $g_{mo} \propto n_D^{1/2}$ and $(-V_{th}+V_{bi}) \propto n_D$, this result is explained by a several times increase in effective channel carrier density. Here, n_D denotes the carrier density in the channel region beneath the gate.

Figure 4 shows drain current-voltage characteristics for the new SWAT FET (structure (C)) with 0.3 μm-long gate. The maximum g_m is as high as 602 mS/mm at 1 V drain bias with 0.7 V gate bias ($V_{th} = -1.45$ V). This value is the highest ever reported for GaAs MESFETs, and still higher than that of a HEMT with 0.33 μm long gate at 77 K (580 mS/mm)[5]. Although the obtained superb performance originated from the lateral diffussion of n^+ dopants to the channel region beneath the gate, the feasibility of GaAs MESFETs as a very high transconductance device was experimentally verified in this work.

Another important point of view is the gate orientation dependence of the GaAs FET characteristics. Figure 5 shows that the gate orientation dependence for the V_{th} shift is essentially the same for the three investigated FET structures, although the V_{th} shift itself is especially stronger for the shorter gate length in structure (C) devices. This fact means that the gate orientation effect is not dominated, but is enhanced by the lateral diffusion of n^+ impurities through the short channel effect.

DYNAMIC BEHAVIOR

In order to examine the dynamic behavior of the new SWAT FET, 25-stage ring oscillators were

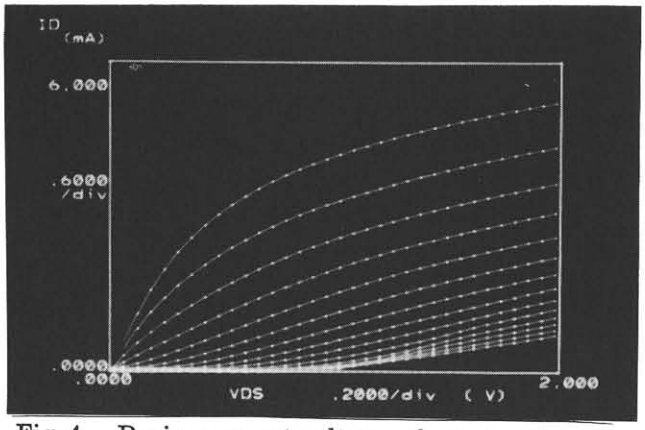

Fig. 4. Drain current-voltage characteristics for 602 mS/mm FET. (n: 30 keV, 3.2×10^{12} cm^{-2}; n^+: 70 keV, 2.5×10^{13} cm^{-2}, $L_g=0.3$ μm, $W_g=10$ μm, $V_g=0.6\sim-2$ V).

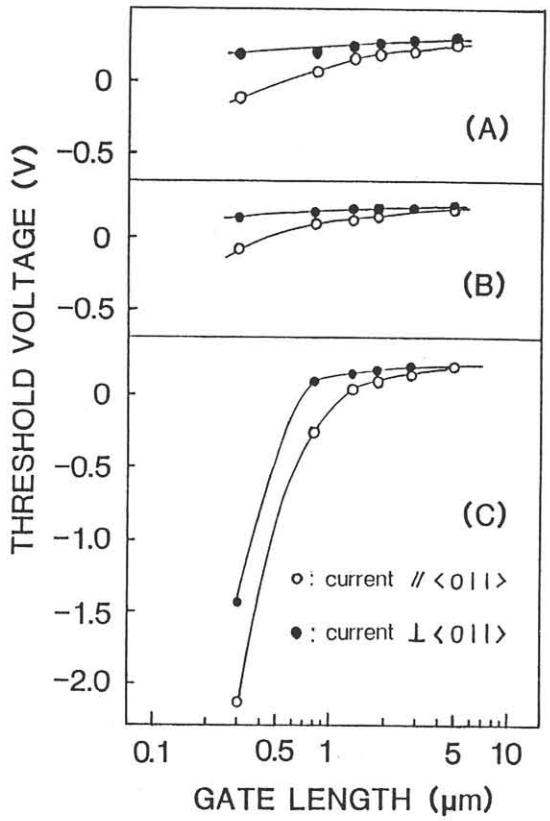

Fig.5. Threshold voltage gate orientation dependence for three SWAT FETs.

fabricated. The basic circuit style is an E/D direct coupled FET logic (DCFL), composed of 0.7 μm-long gate structure (C) FETs. Gate widths are 10 μm for enhancement mode FETs and 5 μm for depletion mode FETs. Average g_m over a 2 inch wafer was 315 mS/mm for enhancement mode FETs.

Drain supply voltage (V_{DD}) dependence of propagation delay time (t_{pd}) and power dissipation (P_d) measured at room temperature are shown in

Fig. 6. At 1 V V_{DD}, 18.4 ps/gate t_{pd} was achieved with very small P_d of 0.59 mW/gate. The minimum t_{pd} was 16 ps/gate at 6 V V_{DD} with 6.7 mW/gate P_d. The output waveform is shown in Fig. 7.

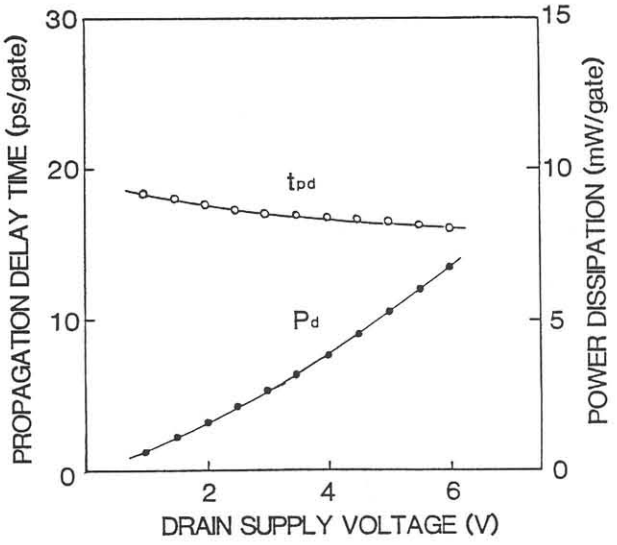

Fig. 6. Propagation delay time (t_{pd}) and power dissipation (P_d) drain supply voltage dependences.

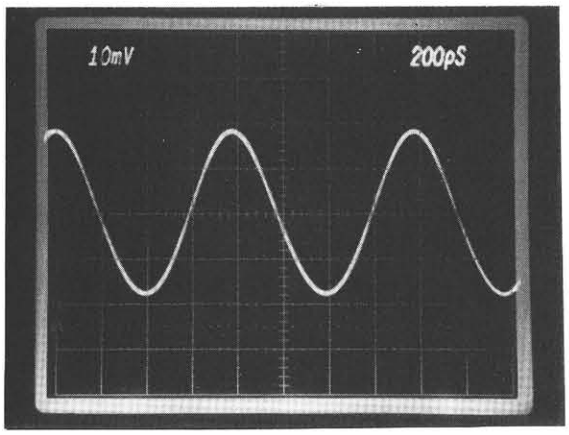

Fig. 7. Output waveform of a 25-stage ring oscillator. (V_{DD}=6 V; t_{pd}=16 ps/gate)

CONCLUSIONS

The highest transconductance (602 mS/mm) GaAs MESFET was fabricated by using a combined SWAT and WSi_x gate n^+ selective implantation technology. Reduction of source series resistance and increase in carrier concentration, caused by the diffusion of dopants, improved the transconductance. Gate length dependence and the gate orientation effect were also investigated in this work. The gate orientation effect turned out to be not dominated but enhanced by the lateral diffusion of the implanted impurities to the channel region beneath the gate electrode. Dynamic behavior for the new SWAT FET was examined by 25-stage ring oscillators. From a 0.7 μm-long gate device, a minimum t_{pd} of 16 ps/gate was obtained.

Through this work, the feasibility of GaAs MESFET as a very high transconductance device at room temperature was experimentally verified.

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