Through-AIN Implantation Technology for 1. 7 ns GaAs 4k×1b SRAM

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A through-AlN implantation technology for fabricating high-K value FETs with sufficiently small scatter in threshold voltage has been developed. Using this technology, several kinds of ring oscillators and a GaAs 4kb static RAM have been fabricated to assess the speed and power performance of 1 μ m gate E/D-DCFL circuits. Propagation delay times were 33 ps/gate and 115 ps/gate for FI/FO = 1/1 and FI/FO = 3/3 with 0.3 mm-long wiring circuits, respectively. A minimum address access time of 1.7 ns was obtained with a total power dissipation of 600 mW. This is the fastest address access time for GaAs 4kb static RAMs ever reported.

(1) Introduction

Development of GaAs ICs has increased remarkably because of demand for high-speed computer and communication systems. Recently, GaAs LSIs, such as a 16 x 16-bit parallel multiplier⁽¹⁾ and 4kb and 16kb static RAMs^{(2),(3)}, have been fabricated successfully, demonstrating the feasibility of GaAs high-speed LSIs. When the circuit complexity increases as in the case of LSI/VLSI, the switching speed is expected to be seriously affected by the wiringrelated capacitance⁽¹⁾. In order to improve the performance of these LSIs and to expand them into VLSIs, it will be necessary to improve the output-current-drive capability of GaAs MESFETs by increasing the transconductance and by reducing the wiring capacitance.

The authors of this paper have reported that through-AlN implantation technology for forming a thin n-channel layer is an effective way to fabricate a high transconductance $FET^{(4)}$. Another way to increase transconductance is to reduce the gate length without the short channel effects which prevents further performance improvement. The short channel effects are influenced by the thickness of the n⁺-layer to form the region of the source and drain as well as the thickness of the channel⁽⁵⁾. Therefore, n⁺-layer formation has a significant role when a gate length is reduced to less than 1.0 µm. In this paper, we will show that further increase of transconductance, with sufficiently small standard deviation in threshold voltage, can be achieved by the through-AlN implantation. We will discuss the effects of short channel effects of the n⁺ implantation energy on the fabricating FETs. We also cover the feasibility of this technology for ultra-fast LSIs by assessing the speed/power performance of ring oscillators and 4kb static RAMs.

(2) Experimental procedures

Experimental procedures for optimizing the thickness of AlN films and implantation conditions in the fabrication of the through-AlN implanted FETs are as follows. First, AlN films of three different thicknesses (10, 20, and 30 nm) were reactive-sputtered on Cr-doped 2-inch LEC GaAs substrates. The thickness variation of AlN film was less than 5 % in a wafer. Si⁺ ion implantation was done at 30 keV through the AlN films. Dosages were intentionally chosen to hold the V_{th} with nearly O V. Annealing was carried out at 850 °C for 15 min. The tungsten-silicide gate, self-aligned GaAs MESFETs were then fabricated(6),(7). The n⁺-layers were implanted at 90, 120 and 175 keV with dosages of 1.0, 1.3 and 1.7 x 10^{13} cm⁻². Conventional self-aligned MESFETs⁽²⁾, using a 59 keV bare-implanted nchannel, were also fabricated with an identical

GaAs wafer for comparison.

(3) Results and discussion

(A) Effect of thickness of AlN film on the performance and uniformity of FETs

Fig. 1 plots the K-value against threshold voltage measured with the parameter of the AlNfilm thickness. It can be seen that K-values of through-implanted FETs are larger than those of conventional FETs, and that K-values increase as the thickness of AlN film increases. The increased K-value should be due to decrease in the effective thickness of the n-channel. In addition, these results imply that the extremely thin channel layers (less than 100 nm) formed with 30 keV through-AlN implantation have retained high quality. Fig. 2 plots standard deviations of the threshold voltage, σV_{th} , against V_{th} with the parameter of AlN-film thickness. It is clear that the through-AlN implanted FETs exhibit smaller $\sigma_{V_{\mathrm{th}}}$ than the conventionally implanted FETs if the thickness of the AlN film is less than 20 nm. The improved uniformity suggests that introduction of surface defects and/or contaminant impurities should be suppressed by the use of AlN film, acting as a surface passivation film through the process of channel layer formation. Furthermore, in the case of the through-AlN implantation FETs, the effective doping concentration of the channel layer is increased⁽⁴⁾ compared to conventional FETs, therefore, threshold voltage is less sensitive to residual impurities. However, it should be noted that $\sigma^{
m V_{th}}$ for through-AlN implantation FET with 30 nm thick AlN is considerably larger than others. In the implantation through 30 nm AlN film, the peakcarrier position is settled at the interface between the GaAs substrate and the AlN film. Therefore, it is expected that V_{th} is greatly affected by factors such as variation of AlN film thickness which varies about <u>+</u>5 % over a 2inch wafer. In fact, it was estimated that this variation caused threshold voltage variation of 43 mV; corresponding to one half of the $\sigma V_{\rm th}$ measured. From the results and discussion of Fig. 2, it was concluded that the main reason for the variation of threshold voltage was the variation of AlN film thickness.



Fig. 1 Averaged K-value as a function of the threshold voltage with the parameter of AlN film thickness.



Fig. 2 Standard deviation of threshold voltage, $\sigma V_{\rm th}$, as a function of the threshold voltage with the parameter of AlN film thickness.



Fig. 3 Gate-length dependence of parameter, N_g, as a parameter of implantation energy for forming the n⁺-layer. N_g indicates the degree of subthresholdcurrent cutoff.

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(B)Role of n⁺ implantation energy on short channel effect

Fig. 3 shows the parameter N_g exhibiting the degree of subthreshold-current cutoff⁽⁸⁾ as a function of the gate length with a parameter of implantation energy for forming a self-aligned n⁺-layer. AlN film thickness for through-implantation was 20 nm, and the peak carrier density for n⁺-regions was held constant by adjusting the dosages of n⁺-implantation. As is apparent from the figure, short channel effects (N_g increase due to decrease in gate length) are reduced for all through-AlN implantation FETs compared with conventional FETs. Furthermore, short channel effects are reduced as the implantation energy for the n⁺-layer is decreased.

Fig. 4 shows K-value as a function of the gate length with a parameter of implantation energy for forming self-aligned n^+ -layers. Note that K-value reductions are less pronounced for all through-AlN implantation FETs compared with conventional FETs. However, K-values for the FETs with 90 keV implantation energy have a tendency to become smaller. This is not only due to the increased effective gate length with decreasing lateral spread for the n^+ -layer but also is due to increase in source series resistance with decrease of implantation dosage for the n^+ -layer. The highest K-value for 1.0 µm gate FET is achieved at 120 keV for n^+ -layer implantation energy.

(C)Speed and power performance of E/D-DCFL circuits

To assess the speed and power performance of E/D-DCFL circuits, several kinds of ring oscillators were fabricated. The n-channel layer of enhancement FETs (E-FETs) were implanted at 30 keV through-20 nm AlN film and the n⁺-layer at 120 keV with 1.7×10^{13} cm⁻². The transconductance measured with a gate-bias voltage at 0.7 V was high at 230 mS/mm for V_{th} = 0.040 V in the gate length of 1.0 µm. The breakdown voltage of the gate was high at 6 V.

In ring oscillators, the gates for the E-FETs were 1.0 μm long and 10 μm wide. For the



Fig. 4 Gate-length dependence of K-value as a parameter of implantation energy for forming the n⁺-layer.



Fig. 5 Oscillograph of oscillation waveforms
 for an unloaded ring oscillator
 (FI/FO = 1/1).



Fig. 6 Photograph of the completed GaAs 4kb static RAM.

depletion FETs (D-FETs) they were 2.0 μ m long and 5.0 μ m wide. Fig. 5 is an oscillograph of oscillation waveforms for an unloaded ring oscillator (FI/FO = 1/1). The propagation delay time was measured as 33 ps/gate with power dissipation of 0.67 mW/gate at V_{DD} = 1.5 V. Loaded delay time was measured as 115 ps/gate at 0.67 mW/gate power dissipation for FI/FO = 3/3 with 0.3 mm-long wiring.

(D) Application to GaAs 4k x 1b static RAM

Using the through-AlN implantation technology, a GaAs 4k x 1b static RAM was fabricated as a test vehicle. Fig. 6 is a photograph of the completed 4kb static RAM. This device consists of E/D-DCFL circuits on a 5.5 mm x 3.7 mm chip in which 26663 FETs are integrated. The gates for the switching FETs are 1.0 µm long. The gates for the depletion load FETs are 4.0 µm long for memory cells and 2.0 μm long for peripheral circuits. The cell size is 47 µm x 32 µm, realized using a minimum design rule of 1.5 µm. To reduce the wiring capacitance, a 2 µm design rule was used for metalizations. X-address access time was measured using a probe card modified for high-speed testing in a 50-ohm measurement system.

Fig. 7 is an oscillograph of X-address input and output waveforms at minimum address access time. A minimum address access time of 1.7 ns was obtained with a total power dissipation of 600 mW. This is the fastest address access time for GaAs 4kb static RAMs ever reported.

(4) Summary

A through-AlN implantation technology for fabricating high-K value FETs with sufficiently small standard deviation in threshold voltages has been described. Typical transconductance was 230 mS/mm for 1.0 µm long gate enhancement FETs. Propagation delay times of DCFL ring oscillators were measured as 33 ps/gate and 115 ps/gate for FI/FO = 1/1 and FI/FO = 3/3 with 0.3 mm-long wiring circuits, respectively. The GaAs 4kb static RAM fabricated using this technique afforded a minimum address access time of 1.7 ns with a total power dissipation of 600 mW. This is the fastest address access time for GaAs 4kb



Fig. 7 Oscillograph of X-address input and output waveforms at minimum address access time.

static RAMs ever reported.

This technology has great promise and will open new avenues for development of high speed GaAs LSIs.

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References

- Y.Nakayama, et al., IEEE J. Solid-State Circuits, vol. SC-18, 599, 1983.
- (2) N.Yokoyama, et al., 1984 ISSCC Digest of Technical Papers, 44.
- (3) Y.Ishii, et al., GaAs IC Symp., 220, 1984.
- (4) H.Onodera, et al., IEEE Trans. Electron Devices, vol. ED-31, 1808, 1984.
- (5) K.Yamasaki, et al., Proc. 14th Conf. Solid State Devices, Tokyo 1982, Jpn. J. Appl. Phys. Suppl. 22-1, 381, 1983.
- (6) N.Yokoyama, et al., 1983 ISSCC Digest of Technical Papers, 44.
- (7) N.Yokoyama, et al., IEEE J. Solid-State Circuits, vol. SC-18, 520, 1983.
- (8) N.Kato, et al., IEEE Electron Device Lett., vol. EDL-4, 417, 1983.