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Advanced GaAs SAINT FET Fabrication Technology and its Application to above 9 GHz Frequency Divider

T. Enoki, K. Yamasaki, K. Osafune, and K. Ohwada

NTT Atsugi Electrical Communication Laboratories
3-1,Morinosato Wakamiya, Atsugi-shi
Kanagawa Pref., 243-01 Japan

An advanced (flat-gate) SAINT FET structure without the excess gate metal overlapping the dielectric film is realized by newly developed planalization technology, and which decreases gate parasitic capacitance. BFL M/S (master/slave) frequency dividers fabricated with this technology operated up to 9.2 GHz at room temperature. It is confirmed that this FET structure is advantageous in high speed and high frequency GaAs ICs.

1. Introduction

High speed GaAs LSIs, such as the 16kb SRAM,[1] have been realized with SAINT FETs.[2] Moreover the short channel effect, which is an obstacle in gate length shortening for much faster operation, was suppressed by a buried P-layer SAINT FET (BP-SAINT FET).[3] Using BP-SAINT FET, operation below 10 ps/gate with E/D ring oscillator, and LSCFL 7.5 GHz 1/4 frequency divider[4] are some of the realized advantages. However, in these SAINT FETs, the gate metal formed by the lift-off method unfavorably overlaps the dielectric film. This excess gate metal increases parasitic capacitances, and degrades high frequency performance. In order to overcome this disadvantage, an advanced (flat-gate) SAINT FET structure without excess gate metal overlapping the dielectric film was proposed and realized by newly developed planalization technology. BFL 1/2 frequency dividers fabricated with this process operated up to 9.2 GHz at room temperature, which is the highest frequency in any semiconductor devices.

2. FET Fabrication Process

Schematic cross-sectional views of a flat gate SAINT FET compared with a conventional SAINT FET are shown in Fig. 1. The flat-gate SAINT process is almost the same as the conventional SAINT process except gate formation. A gate electrode formation of a flat-gate SAINT is described below.

After opening the gate contact region, Mo/Au is deposited onto the whole surface by sputtering (Fig. 2(a)). Then, the Au surface is planalized by ion beam milling with a large ion beam incident angle, until Au remains only in the gate dip region (Fig. 2(b)). This planalization method accounts for the cosθ dependence of Au etching rate on the ion beam incident angle (θ). Then the

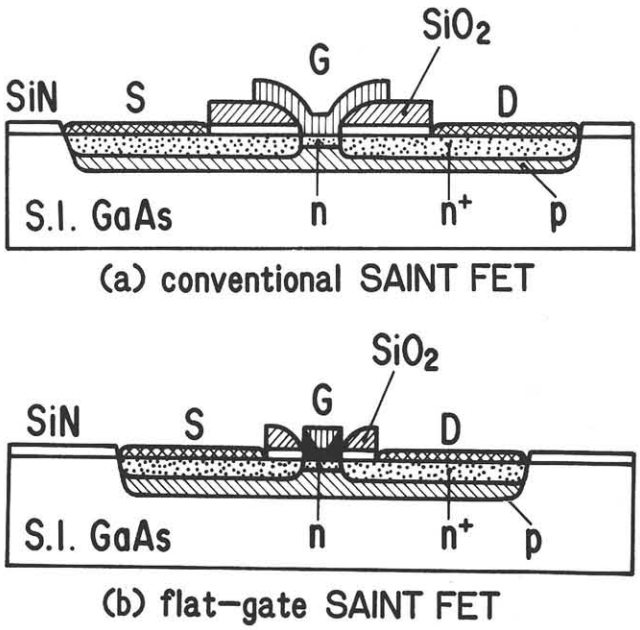

Fig. 1 Schematic cross-sectional views of
(a) conventional SAINT FET
(b) flat-gate SAINT FET.

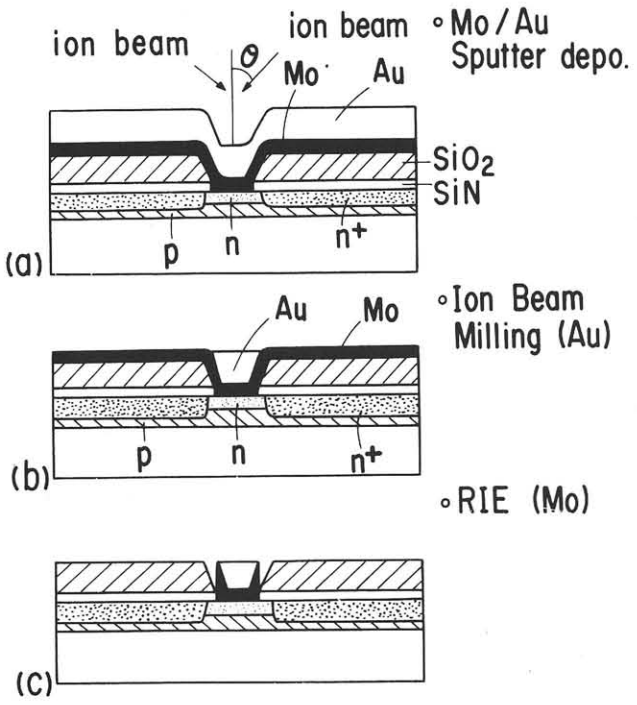

Fig. 2 Gate formation process of a flat-gate SAINT FET.

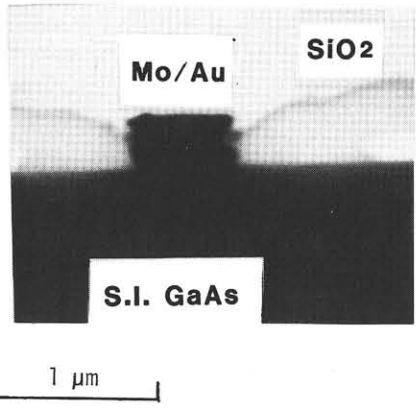

Fig. 3 A SEM photograph around the gate of a flat-gate SAINT FET.

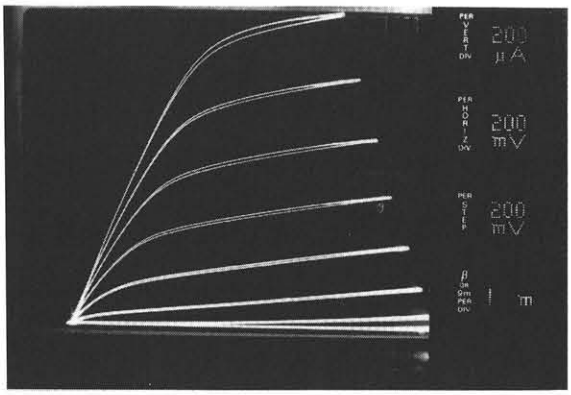

Fig. 4 I-V characteristics of a flat-gate SAINT FET. L_g=0.5 μm, W_g=10 μm, V_g=0.0~-1.4 V.

Au pattern is replicated in the Mo layer by Reacive Ion Etching (RIE). Consequently, the gate electrode is embedded only in the gate opening region. A SEM photograph around the gate is shown in Fig. 3. Finally, ohmic electrodes (AuGe/Ni) are formed (Fig. 1(b)).

With this gate electrode formation, 0.5 μm-gate length FETs were realized without the excess gate metal overlap .

Active layers (n- and n^+-layers) were provided by selective Si^+ implantation at 30 keV with a dose of 8.5×10^{12} cm^{-2}, and at 200 keV through 0.15 μm SiN film with a dose of 4×10^{13} cm^{-2}. The p-layer was selectively buried under the active layers by Be^+ implantation at 70 keV with a dose of 6×10^{11} cm^{-2}.

3. FET characteristics

The I-V characteristics of flat-gate SAINT FET with 10 μm-width and 0.5 μm-length gate are shown in Fig. 4. The average values for device parameters derived from the I-V characteristics are summarized in Table 1. Static characteristics almost the same as those of a conventional SAINT FET are realized by this process without the damage in ion beam milling and RIE.

To estimate the gate capacitances of the FET, the S-parameter of an FET with 200 μm-width and 0.3 μm-length gate was measured. The gate-drain capacitance (C_{gd}) derived from $Im(-Y_{12})$ are shown in Fig. 5, in comparison with that of a conventional SAINT FET. C_{gd} is decreased by 26 fF/200 μm-gate-width. This C_{gd} reduction is considered to be due to the removal of the excess gate metal overlapping the dielectric film.

The frequency dependence of the current gain (H_{21}) is shown in Fig. 6. According to Fig.6, cut-off frequencies (f_T) of a flat-gate and conventional SAINT FET are 32 and 24 GHz, respectively. This advantage is due to the reduction of the gate parasitic capacitances.

	flat - gate	Conventional
Gate metal	Mo/Au	Ti/Pt/Au
Gate length (μm)	0.5	0.5
V_{th} (V)	− 1.1	− 1.3
gm (mS/mm, V_g=0V)	184	180
Barrier height (eV)	0.71	0.78
K ($mA/V^2/mm$)	114	92

Table 1 Average values for characteristics of SAINT FETs.

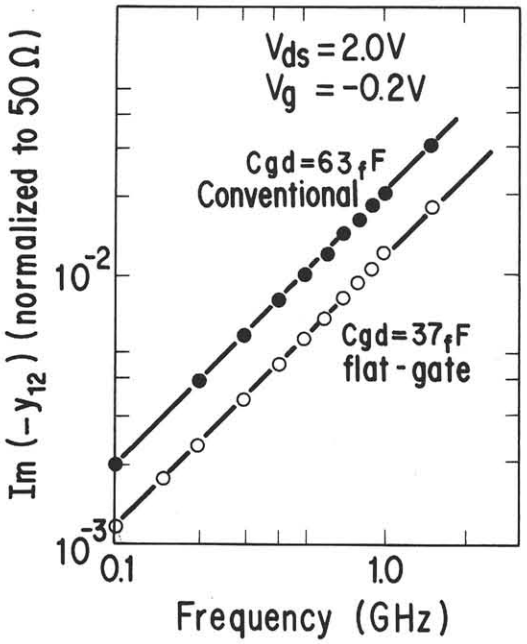

Fig. 5 Frequency dependence of $Im(-Y_{12})$ C_{gd} derived from $Im(-Y_{12})$ of a conventional and a flat-gate SAINT FET (L_g=0.3 μm, W_g=200 μm) are 63, 37fF, respectively.

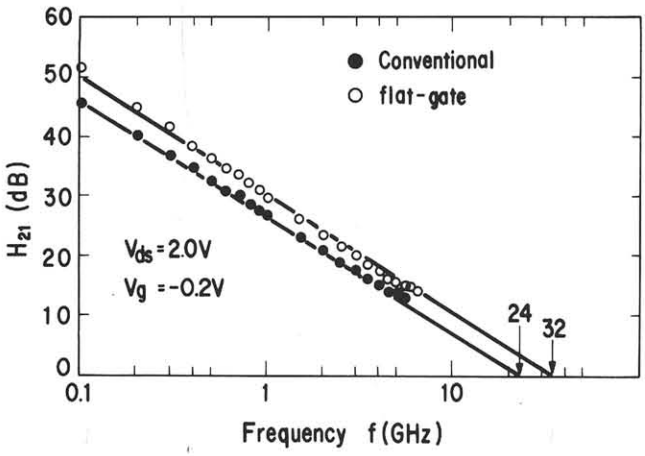

Fig. 6 Frequency dependence of the current gain. Cut-off frequency of a conventional and a flat-gate SAINT FET are about 24 and 32 GHz, respectively. (L_g=0.3 μm, W_g=200 μm)

4. BFL ring oscillator

In order to confirm the high speed operation of the flat-gate SAINT FET, 17-stage BFL ring oscillators were fabricated by the flat-gate SAINT process. The gate length and width are 0.5, and 20 μm, respectively. The distribution of propagation delay time (t_{pd}) and power dissipation (P_{dis}) in a 2-inch wafer measured at room temperature are shown in Fig. 7, compared with that of conventional SAINT ring oscillators. Power dissipation dependences of propagation delay time are simulated by the use of SPICE II with gate parasitic capacitances ($2C_p$). According to this simulation, C_p of flat-gate SAINT FETs decrease by 4.5 fF/20 μm-gate-width. Considering the difference of FET patterns and the accuracy of the S-parameter measurements or the simulations, this amount of reduction is reasonable, compared with the results of RF measurements. The minimum propagation delay time measured at room temperature is 29.4 ps/gate (25.2 mW/gate).

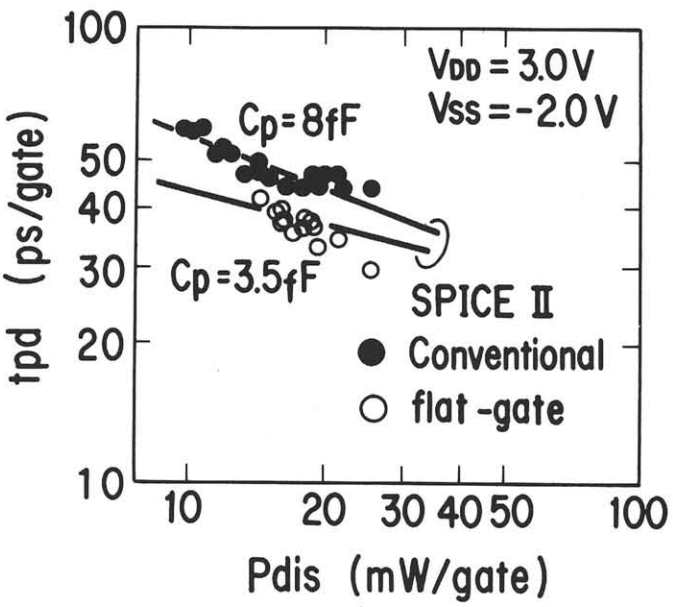

Fig. 7 Propagation delay time versus power dissipation for 17-stage BFL ring oscillators. These relationships are simulated by the use of SPICE II with gate parasitic capacitances ($2C_p$). C_p of a flat-gate SAINT FET decreased by 4.5 fF/20 μm. (L_g=0.5 μm, W_g=20 μm)

5. BFL 1/2 frequency divider

The flat-gate SAINT process is applied to fabrication of a binary frequency divider with a BFL dual clocked master/slave flip-flop.[5] The

gate length and width are 0.5 and 40 μm, respectively. The distribution of maximum toggle frequencies ($f_{tog.max}$) for standard biases (V_{DD}=3.0 V, V_{SS}=-2.0 V) in a 2-inch wafer are shown in Fig. 8. Average $f_{tog.max}$ of conventional and flat-gate SAINT dividers are 5.2 and 7.4 GHz, respectively. Operating frequency of a flat-gate SAINT divider rises above 2 GHz, compared with that of a conventional SAINT divider. Operation at 9.2 GHz (power dissipation of 290 mW) was achieved by optimizing bias voltages. The operating waveform is shown in Fig. 9.

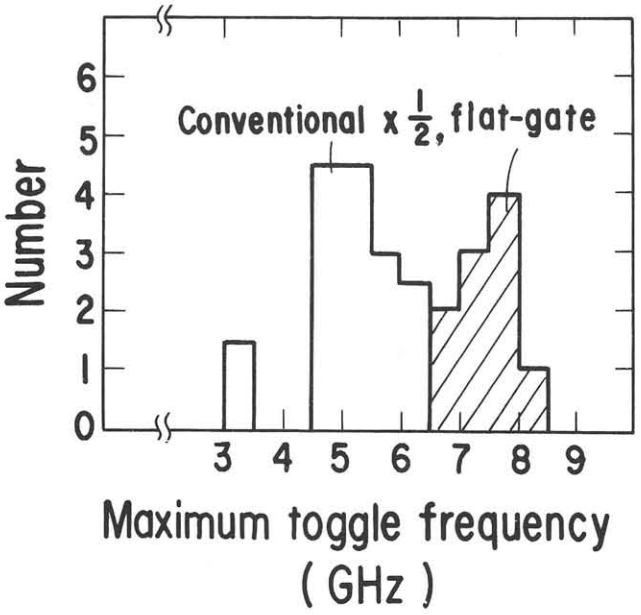

Fig. 8 The distribution of maximum toggle frequencies in 2-inch wafer for standerd biases (V_{DD}=3.0 V, V_{SS}=-2.0 V). Average $f_{tog.max.}$ of conventional and flat-gate SAINT dividers are 5.2 and 7.4 GHz, respectively. (L_g=0.5 μm, W_g=40 μm)

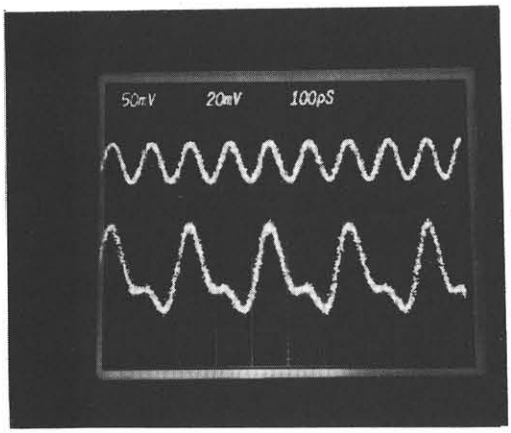

Fig. 9 Response waveform of the binary frequency divider operating at 9.2 GHz (power dissipation 290 mW). Clock Input: 0.7 V(peak-peak), Output: 83 mV(peak-peak).

6. Conclusion

A flat-gate SAINT FET structure without the excess gate metal overlapping the dielectric film successfully realized by newly developed planalization technology by the use of ion beam milling with a large incident angle of ion beam. This FET structure enable to decrease gate parasitic capacitances by about 0.13-0.23 pF/mm , according to the result of ring oscillator and RF measurements. The binary frequency deviders using the flat-gate SAINT FET have successfully operated up to 9.2 GHz, which is the highest frequency in any semiconductor devices at room temperature.

In conclusion, the flat-gate SAINT is advantageous in high speed and high frequency GaAs ICs.

7. Acknowledgements

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References

(1) M.Ohmori:11th international symposium on gallium arsenide and related compounds, Biarritz,(1984).

(2) K.Yamasaki,K.Asai,T.Mizutani, and K.Kurumada:Electron.Lett.,18,(1982), pp.119-121.

(3) K.Yamasaki,N.Kato, and M.Hirayama: Electron.Lett.,20,(1984),pp.1029-1031.

(4) T.Takada,M.Togashi,M.Idda,K.Yamasaki, and K.Hoshikawa:Paper of Tech. Group on Solid State Devices,IECE Japan,TGSSD84-116, (1985),pp.97-104.

(5) K.Osafune,K.Ohwada, and N.Kato:Paper of Tech.Group on Solid State Devices,IECE Japan,TGSSD84-118,(1985),pp.113-118.