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# 6-7 GHz GaAs IC's with High Yield 0.5 μm Gate-Length SAINT

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High speed GaAs integrated circuits fabrication technology with 0.5 μm gate length is described. Its newly developed features are (i) buried p layer SAINT with Si 30 keV ion implantation , (ii) use of low dislocation density wafers, and (iii) highly uniform 0.5 μm lithography. 1/4 frequency dividers show toggle frequencies of 6-7 GHz with 97% yield.

## 1. Introduction

The potentiality of GaAs IC/LSIs for use in gigabit rate digital communication systems and high speed computers is widely recognized. Presently even commercial GaAs chips with 1 μm gate length are becoming available.

Recently we have developed a process featuring a 1 μm gate length and a 1.5 μm line-and-space rule using stepper lithography and reactive ion etching. Furthermore we applied and evaluated low etch pit density wafers and showed that FET threshold voltage deviation was suppressed to 20 mV for the 1 μm gate length. A 16 Kb RAM(1) was a fruitful accomplishment of these technologies.

Currently, Si bipolar technology(2) has become more competitive than before. We also have worked on the enlargement of FET drivability to achieve high speed ICs. Our approach has been a submicron gate length MESFET with a buried p layer underneath to suppress the short channel effects. The buried p layer SAINT(3) (BP-SAINT) exhibited less than 10 ps/gate delay in a ring oscillator and confirmed its LSI feasibility through the realization of time switch LSI(4).

Problems associated with 0.5 μm BP-SAINT have been (i) lack of optimization for shallow active layer formation and (ii) threshold voltage scatter due to short gate length. The purpose of this paper is to present optimization and evaluation of the shallow active layer and to characterize the lithography and low EPD wafers for 0.5 μm process to understand yield improvement.

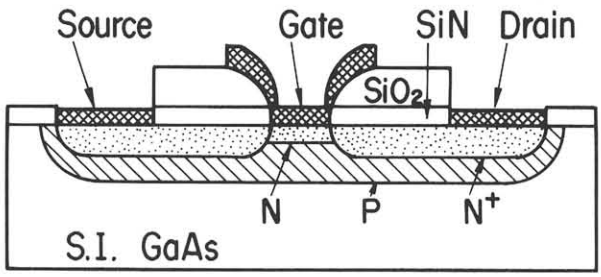



Fig.1 Schematic of buried p layer SAINT FET.

## 2. 0.5 μm Device Process

### 2.1 Shallow Ion Implantation

The most important FET parameter in realizing a high speed IC is transconductance ($g_m$). It has been predicted that $g_m$ can be increased by shallowing the channel depth. The buried p layer SAINT FET is schematically shown in Fig. 1. The p layer was introduced to suppress the substrate current. The depth and concentration of the p layer are so chosen that the built-in depletion should extend across the whole p layer. The first version of a buried p layer SAINT FET was fabricated with 67 keV Si ion implantation for the n layer and 97 keV Be implantation for the p layer(4). The FET with a $V_T$ of 0 V exhibited improved $g_m$'s of typically 170 mS/mm probably due

to the introduction of the p layer that effectively reduces the channel thickness. For the shallower n layer implantation with 30 keV, the thickness of the p layer and $n^+$ layer should also be reduced in accordance with the n layer. However in this experiment, the $n^+$ layer was not actually shallowed according to the scale-down law since the shallowing the $n^+$ layer badly affects the series resistance ($R_s$) and thus the $g_m$. With a fixed $n^+$ layer implantation of 200 keV, an optimized p layer implantation energy was estimated to be 77keV for the 30 keV n layer. Figure 2 clearly demonstrates the $g_m$ increase in the shallow implantation. In the figure the $g_m$ are plotted against the FET threshold voltage($V_T$) for two energies. The $g_m$ was taken under the condition of 1 V drain voltage and 0.5-0.6 V gate voltages. The improvement factor was 1.3 at 230 mS/mm of $V_T$=0V. The $g_m$ improvement factor was less than the expected one from the scale-down law. This was because neither the $n^+$ nor the p layers are shallowed in proportion to the n layer.

2.2 Annealing Optimization

Post-implant activation was carried out using a thermal furnace flowing inert gas. The wafer cap for protection was a 0.15 μm thick SiN film formed by a plasma assisted CVD system.

To set the optimized annealing temperature for a shallow 30 keV n layer, SAINT processed wafers were annealed at temperatures ranging from 700°C to 800°C. Figure 3 shows $g_m$ vs $V_T$ relationships. The results exhibit that 800°C, the long established annealing temperature for 67 keV process give the highest $g_m$. This agrees well with the $n^+$ sheet resistance results in Fig.4. Here Si implantation for the $n^+$ layer was done through a 0.15 μm SiN at 200 keV with a dose of $4x10^{13}cm^{-2}$. Anneal time was 10 minutes. This experiment presents the facts that the thermal annealing temperature for $n^+$ layer has an optimum point at 800°C and that the best $g_m$ can be obtained at the minimum sheet resistance for $n^+$ layer. This means $R_s$ plays a major role.

2.3 0.5 μm Photolithography

Delineation of each photo process step was accomplished using a 10:1 stepper. Main features

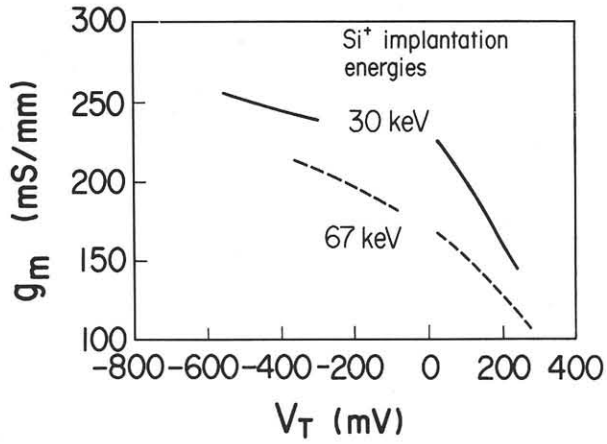



Fig.2 $g_m$-$V_T$ relationships for two n layer ion implantation energies.

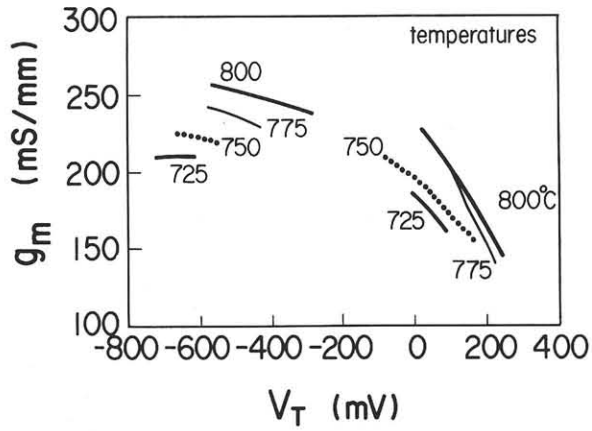



Fig.3 $g_m$-$V_T$ relationships for various annealing temperatures.

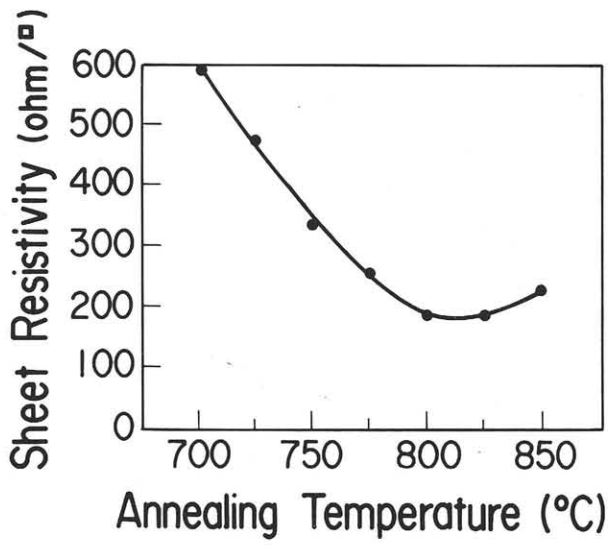



Fig.4 $n^+$layer sheet resistivity against annealing temperatures.

of this lithographic process are (i) there is no resist defect as in contact printing,(ii) highly uniform pattern definition, (iii) extremely precise automatic alignment using a laser assisted stage positioning. These features permit highly critical pattern layout such as 0.5 μm source-gate metal separation, 2.5 μm source-drain separation and 0.5 μm gate metal overlay width and allow realization of high performance FETs with high yield .

Figure 5 is a histogram of gate lengths in a 2 inch wafer compared with conventional contact printing. Using the stepper a small gate length scatter of 0.03 μm was obtained for a 0.5 μm gate length. The SAINT permits submicrometer gate length since the gate is defined by etching.

2.4 Uniformity Evaluation for 0.5 μm BP-SAINT

One of the most significant problems in GaAs LSI has been the scatter of FET characteristics that were affected by crystal defects. With the technologies described here BP-SAINT FETs fabricated on a full 2" wafer showed a $V_T$ standard deviation of 30-40 mV even for half micron gate length.

3. Device Performance

1/4 frequency dividers adopting Low power Source Coupled FET Logic [4](LSCFL) were fabricated and evaluated. It is composed of an ECL compatible input buffer, 2 flipflops, and an output buffer. The total number of FETs, diodes and resistors is 76. Figure 6 is a photomicrograph of the circuit. The chip size was 0.6 mm x 0.85 mm. FET gate length and width are 0.5 μm and 20 μm respectively. The frequency dividers were measured at their designed supply voltages on four wafers. Figure 7 shows a toggle frequency histogram comparing the processes using 67 keV and 30 keV ion implantation energies (in the following chapter these are referred to as version II and version III). The 1/4 dividers using the process of version II operated at the maximum toggle frequency range of 5.2-6 GHz. In contrast to this, for dividers using the version III, all the successful chips operated in the 6-7 GHz range. The success chip yield was considerably high 97% in four wafers. A failed chip was due to bridging pattern defect in the second layer interconnect between a bias line and a signal line. The bridging was probably caused by dust caught on the wafer and replicated into the second layer interconnect.

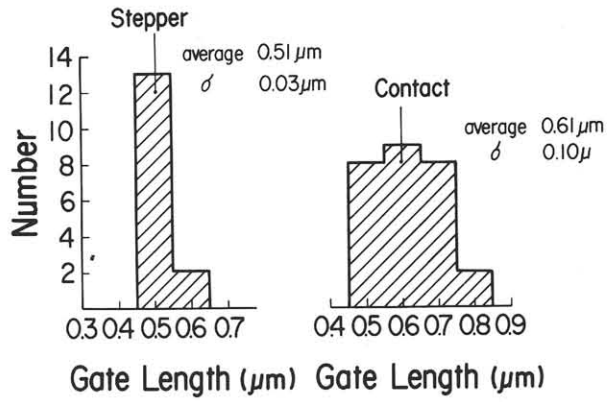



Fig.5 Gate length histogram.

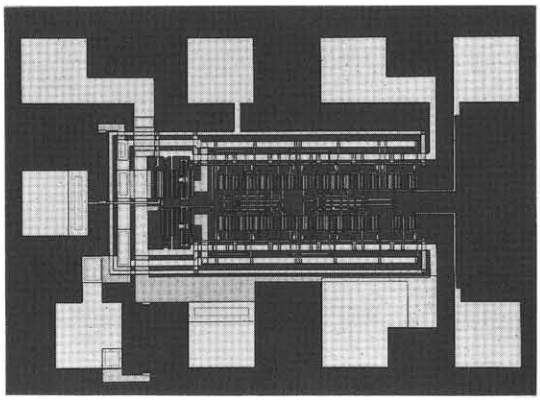


Fig.6 Photomicrograph of 1/4 LSCFL frequency divider

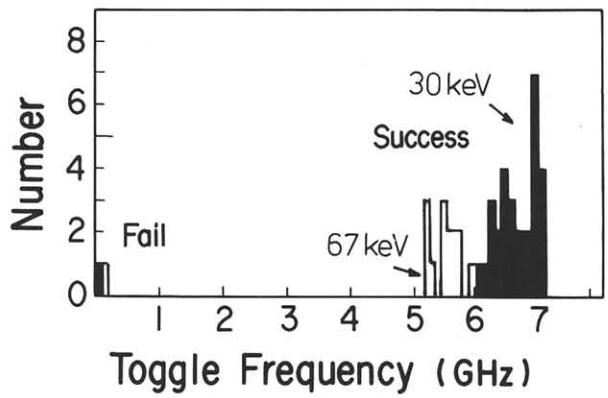



Fig.7 1/4 divider toggle frequency histogram obtained from four wafers using 30-keV n layer ion implantation(closed histogram). The same circuits are compared using 67 keV ion implantation(open histogram).

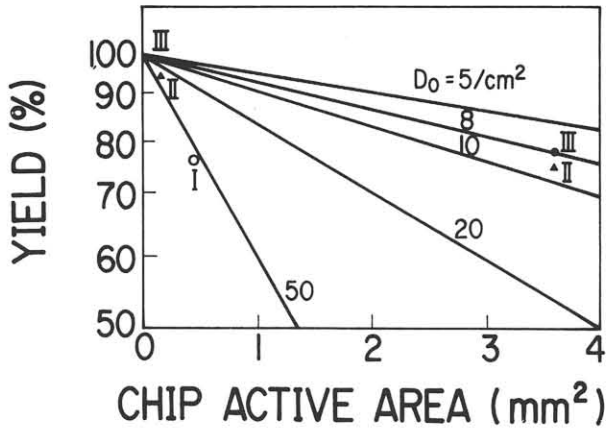
## 4. Discussion and Summary

We feel that the GaAs process has reached the stage of maturity that could provide satisfactory yield of circuits. So far NTT has published chip yield data for several MSI-LSI level complexities[4],[5]. In general, the yield can be discussed for a mass production line which has a large process tolerance. However, we can sometimes utilize the yield to evaluate improvements in the fabrication process.

The published yield data and the latest results are shown in Fig. 8. All of these plotted here adopt the SCFL configuration. Circuits with larger complexities naturally have lower yields. To clarify the stage of improvements for various circuit complexities, the solid lines assuming the Poisson distribution $Y=e^{-D_0 A}$ were also shown, where $D_0$ is randomly distributed defect density of any type , and A is the active chip area. The defects can be attributed to dust, scratches, non-uniformity in $V_T$ or other local abnomalities in device parameters[6]. A process with a small $D_0$ can be considered an improved process.

Advancement from version I to version II is based on the application of low EPD wafers and the use of stepper lithography. The low EPD wafers effectively reduced the scatters in FET threshold voltages and the resistance values in ion implanted resistors. The stepper is also effective since it eliminates resist stripping defects common in contact printing. No significant difference has been observed for versions II and III. However, version III is considerably superior since it is able to produce faster ICs.

In conclusion, the latest technology which led to the high-yield, high-speed logic circuits has been described.Its essential features are high $g_m$ with a shallow active layer, superior uniform, defectless stepper lithography, and the application of low dislocation density wafers. The LSCFL 1/4 divider circuits operated in the 6-7 GHz range with a high success yield. The technology described here will be promising for production of ultra high speed GaAs IC/LSIs.




| Version | Process | Lg | Lithography | n-Layer | Wafer |
|---|---|---|---|---|---|
| I | SAINT | 0.8μm | Contact+EB | 67 keV | Conventional LEC |
| II | BP-SAINT | 0.55μm | Stepper | 67 keV | Low EPD LEC |
| III | BP-SAINT | 0.5μm | Stepper | 30 keV | Low EPD LEC |

Fig.8 Yield vs. chip area relationship for three processes.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