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Absence of Side-Gating in InP MISFET Integrated Circuits

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It is shown that InP MISFETs are virtually free from side-gating effect under normal dark operating condition. In order to understand the difference in the side-gating behavior between InP MISFETs and GaAs MESFETs, a detailed study on the surface I-V characteristics was carried out. It is concluded that the difference is because of the low surface state density in InP.

1. Introduction

In compound semiconductor LSI/VLSIs, failure of device isolation due to surface electrical breakdown and device interference is anticipated to impose a serious limitation on the achievable packing density. In GaAs MESFET IC's, device interference is caused by the side-gating phenomenon [1-3] where the FET drain current starts to be modulated by the voltage on the adjacent ohmic electrode when it exceeds a certain threshold value. It was found by Lee et al that surface breakdown and side-gating were related to each other and this correlation was explained in terms of the bulk-trap filling by bulk space charge limited current[1]. However, our detailed experiments strongly indicated involvement of surface states and we recently proposed a new model for surface breakdown and side-gating[3].

On the other hand, although small scale integration of high speed InP MISFETs[4,5] as well as an excellent performance as microwave power devices[6] have been reported, there has been no report on the side-gating behavior of the InP MISFET. The purpose of the present paper is to investigate the side-gating behavior of the InP MISFET in order to assess its suitability for high-density LSI/VLSIs. Since the InP surface is known to possess a lower density of surface states than the GaAs surface, study of side-gating behavior should also provide a good test for the validity of the above mentioned model.

2. Experimental

InP depletion mode (D-) MISFETs were fabricated on Fe doped LEC semi-insulating InP substrate. The MISFET gate insulator was anodic Al_2O_3/native oxide double-layer produced by the AGW electrolytic anodization process[5]. GaAs D-MESFETs were also fabricated using MOVPE grown epitaxial layer on undoped LEC substrates for direct comparison of the side-gating behavior, using the same photomasks. The device structures and the electrode patterns are shown in Fig.1.

Leakage current characteristics between two ohmic electrodes formed on Fe doped LEC semi-insulating InP substrates were also studied. Alloyed Au/Ge ohmic contacts with different spacing were formed on the InP surface by a standard

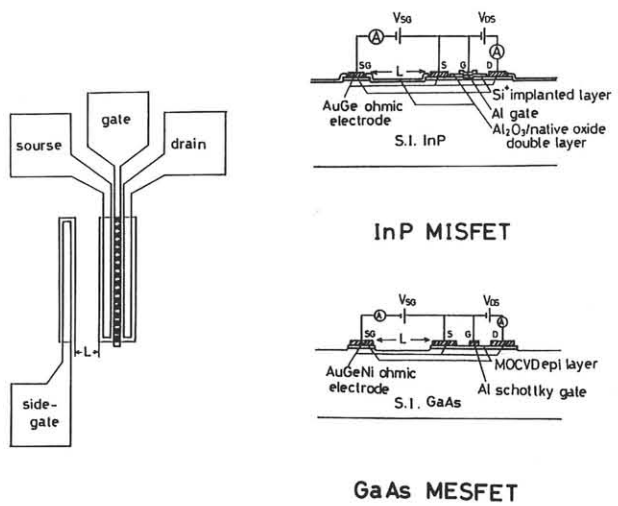

Fig.1 Device structure and electrode pattern used for comparison of side-gating behavior.

photolithographic process. In order to investigate the effect of surface passivation films, various dielectric films including SiO_2, Si_3N_4 and anodic native oxide of InP were formed on the surface. SiO_2 and Si_3N_4 were formed by plasma CVD processes using $SiH_4+O_2+N_2$ and SiH_4+N_2 gas mixtures, respectively, at 300 C. Anodic native oxide films were produced by the same anodization process as used for MISFET fabrication.

3. Experimental Results and Discussion

3.1 Side-gating behavior of InP MISFETs

Figure 2 shows the observed side-gating behavior in the dark of the InP MISFET and GaAs MESFET having the same electrode geometry. As seen in Fig.2, InP MISFETs showed very little side-gating, if any, up to an average field of 30-40 kV/cm beyond which a permanent short-circuit between the side-gate and source took place. On the other hand, GaAs MESFETs always showed a very large reduction of drain current at an average field of about 1-3 kV/cm under negative side-gate bias. The side-gating threshold was found to be equal to the surface breakdown voltage between the side gate and the source. Visible white light emission with uniform or spotty pattern was observed at the outer edge of the source electrode after the onset of side-gating.

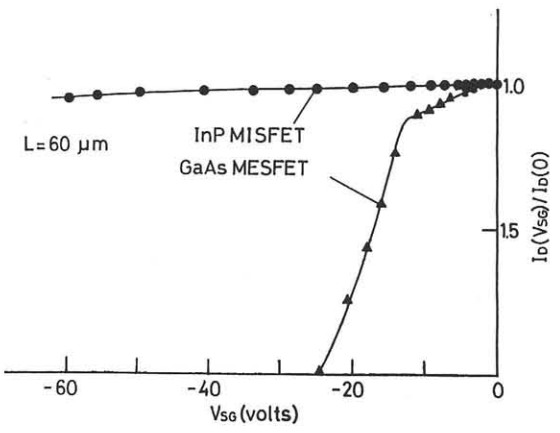

Fig.2 Comparison of side-gating behavior of InP MISFET in the dark. For comparison behavior of GaAs MESFET is also shown. Note that InP MISFET is virtually free from side-gating.

However, when the devices were illuminated by a tungsten lamp, both devices showed similar marked reduction of drain current under negative side-gate bias as shown in Fig.3.

The measured I-V characteristics between the side-gate and source electrode are shown in Fig.4 for both devices. These results strongly indicates that the side-gating is controlled by the bulk leakage current.

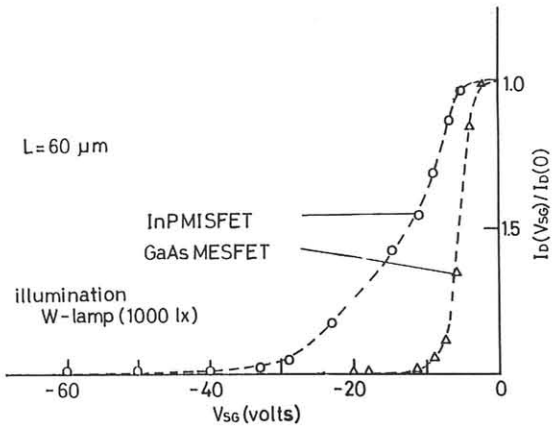

Fig.3 Side-gating behavior of InP and GaAs FETs under illumination.

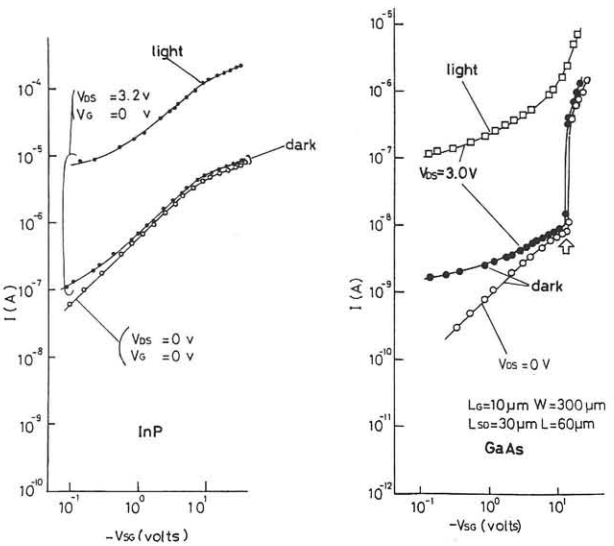

Fig.4 I-V characteristics between side-gate and source electrode for InP MISFET and GaAs MESFET

3.2 Surface I-V Characteristics of Fe doped Semi-insulating InP Substrates

Bearing in mind the close correlation between surface breakdown and side-gating in GaAs MESFETs

[1,7], surface I-V characteristics of InP substrates were investigated in detail. I-V characteristics of unpassivated InP surfaces are shown in Fig.5. For comparison, a typical I-V characteristic of unpassivated GaAs surface is also shown by the dashed curve. The leakage current of InP shows ohmic behavior up to 10-30 kV/cm after which InP permanently breaks down. This behavior is in contrast to the GaAs case[7] where a steep and reversible breakdown takes place at an average field strength of 1-3 kV/cm. A comparison of the breakdown voltage between InP and GaAs surfaces is given in Fig.6. The breakdown voltage of InP is at least about one order of magnitude higher than that of GaAs. In the case of GaAs, white light emission was observed from the anode edge after the onset of the reversible breakdown, whereas no visible light emission took place at the irreversible break down of InP surface.

A more detailed dependence of ohmic leakage current on the electrode spacing is given in Fig.7 (a) in terms of ohmic resistance R_m per unit width of electrode. The resistance calculated by conformal mapping [7] using bulk resistivity is also shown in Fig.7 (a) (R_b). The resistivity of the InP substrate InP was 7.7×10^7 ohm.cm which were separately measured using a sandwich structure. The difference in the ohmic leakage current between InP and GaAs unpassivated surfaces in Fig.5 is basically due to the difference of the bulk resistivity between the two. As seen in Fig.7 (a), the measured ohmic resistance is sensitive to the processing conditions, and could be 1-3 orders of magnitude smaller than the value expected from the bulk resistivity. A similar but even more pronounced sensitivity to passivation conditions was also observed in the case of passivated GaAs surfaces. However, the detailed dependence of the resistance on the electrode distance is very different. While passivation induced low

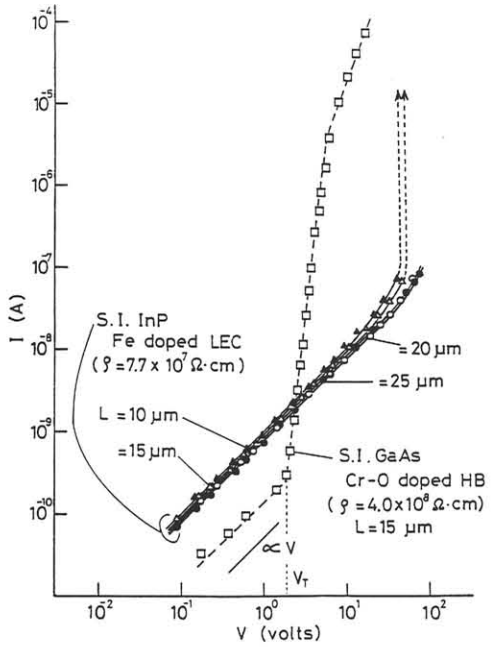

Fig.5 I-V characteristics between ohmic electrodes formed directly on semi-insulating substrates.

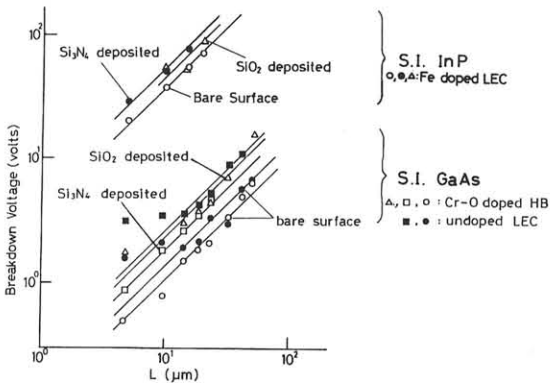

Fig.6 Breakdown voltage versus electrode spacing showing linear dependence.

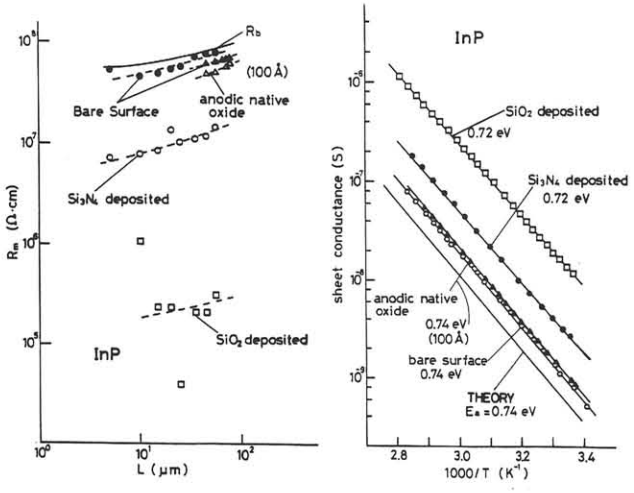

Fig.7 (a) Dependence of ohmic leakage current on the electrode spacing in terms of ohmic resistance R_m per unit width of electrode. (b) Temperature dependence of ohmic leakage current.

resistance showed linear dependence on distance in GaAs[7], indicating formation of surface conduction channel, parallel downward shifts of curves with the same dependence of distance is seen here, expect for the case of the thick anodic oxide which is known to be conductive. This indicates that passivation induced increase of leakage current in InP is due to change of bulk resistivity near surface, rather than formation of surface channel. Measured temperature dependence of ohmic leakage current is shown in Fig.7 (b). In the case of GaAs, the activation energy of the ohmic current was found to be sensitive to the processing condition, and extremely low values of activation energy which characterize surface states in GaAs MIS structures, were characteristics were observed, strongly indicating that the surface channel is due to high density surface states. On the other hand, leakage current in the case of InP has almost the same activation energy as that of bulk, even when the leakage current is much larger than the value expected from the bulk resistivity. This again strongly indicates change of bulk resistivity near the surface caused by various processing rather than the formation of a surface conduction channel.

3.3 Discussion

The observed remarkable difference in side-gating behavior between InP and GaAs can be best explained by our new model for the surface breakdown and sidegating in GaAs MESFETs[3], where field concentration due to surface state filling causes avalanche breakdown, and the resultant electron current injected into bulk changes the occupation function of bulk deep traps underneath the device. On the other hand, due to low density of surface states at the anodic native oxide-InP interface as demonstrated by C-V measurements, surface I-V characteristics of InP are dominated by bulk traps near the surface, as confirmed by the present detailed study. Therefore a premature surface breakdown due to surface state filling is avoided, leading to the absence of side-gating.

Appearance of side-gating under illumination is because the photo-excitation producing bulk leakage currents flow in both materials in a similar way as evidenced by the experiment, and these currents change the occupation function of the deep traps under the channel whose density has a similar magnitude in both materials.

The present observation combined with the higher driving capability of InP MISFETs as compared with GaAs MESFETs and HEMTs, indicates that InP is a superb material for highly packed compound semiconductor LSI/VLSIs.

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