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Abrikosov Vortex Memory with Novel Cell Structure

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A nondestructive readout random access memory cell based on the use of Abrikosov vortices in thin-film type-II superconductors is newly designed and experimentally tested. The cell occupies an area of 30 x 60 μm^2 with a 5-μm design rule. Proper memory cell operation is achieved in the so-called 1,-1 mode using the shift saturation effect which occurs on the characteristics of the write currents vs. the shift value of the sense gate threshold curves. This is the first Abrikosov vortex RAM cell to operate properly. The write current level has been reduced one order of magnitude using a Pb/In/Au film co-evaporated at 90 K for the vortex storage region.

1.Introduction

An Abrikosov vortex memory, in which vortices in type-II superconductor thin films are used as information bits, is attractive because its vortex size is smaller than that of persistent current-type superconductive memories.[1)2)]

A vortex file memory having a bubble memory type structure has been proposed by Bächtold.[3)] In addition, Uehara et al.[4)] have proposed a trapped vortex memory. This represents the first random access memory cell utilizing vortices trapped in a type-II superconductor thin film. This memory cell has potential application in high-capacity RAMs because of its small cell size and simple structure. They have also reported preliminary experimental results on vortex generation and detection. However, their memory has not yet to exhibit stable operation characteristics. This is because there exist many difficulties such as large write current levels, a narrow write operation margin, and a fail operation on "0" writing in the "0" memory state.

This paper proposes an improved vortex memory cell structure and a novel memory operation mode which help to avoid the difficulties inherent in the cell proposed by Uehara et al. Experimental results in which stable memory operation has been confirmed are also reported.

2.Memory cell structure

A schematic structure of the improved Abrikosov vortex memory cell is illustrated in Figure 1. The main difference between the previously reported cell and this one is the location of the sense gate (SG). The SG in our vortex memory is located on the thick superconductor near the edge of the vortex storage region (VSR). In the previously reported cell structure, however, it was located directly on the VSR.

A two-junction SQUID gate was also used for the SG in our cell instead of a single Josephson

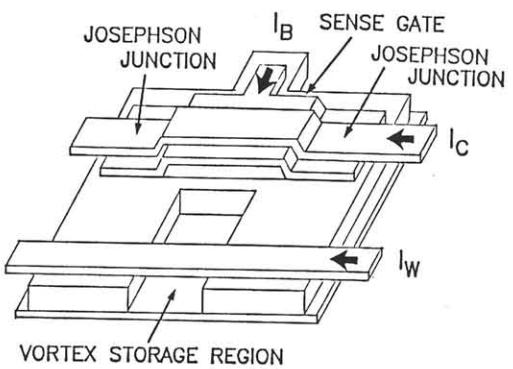

Fig. 1 Schematic structure of Abrikosov vortex memory cell. I_W is write current for generating information vortices, I_B is Josephson junction bias current for reading out vortices, and I_C is control current of sense Josephson gate.

junction taking advantage of its high magnetic field sensitivity. Vortices are generated in the type-II superconductor thin film by the magnetic field associated with the current passing through write control lines, which run along the edge of the VSR. The thin film in this region has a reduced thickness to allow vortices to enter into the region more easily.

3.Operation principle

The previously reported memory cells were operated in the so-called 1,0 mode, in which the vortex storing state indicates "1" state and the non-vortex state indicates "0" state. A "0" writing operation is carried out by canceling the stored vortices with an equal number of opposite sign vortices. These vortices are generated by an opposite sign write current. However, when the write current fluctuates around the nominal value and/or the vortex pinning force is large in the VSR, the "0" writing operation is incomplete since excess vortices remain in the VSR. These excess vortices are accumulated during the write operation cycles.

The operation instability in the previously reported cell is caused by these accumulated vortices. To avoid this instability, we employed the so-called 1,-1 operation mode in our memory cell, in which the vortex storing state also indicates "1" but the opposite sign vortex storing state indicates "0". The stored vortices can be eliminated by generated vortices having opposite signs. Additionally, the excess opposite sign vortices are stored in the VSR indicating the "0" state.

In this operation mode, it is necessary to distinguish the memory states of the cell by detecting the polarity of the stored vortices. This is possible by detecting the shift direction of the SG threshold curves after "1" or "0" writing. In the previously reported cell, however, Josephson current, I_J, suppression of the SG characteristics as well as the shift of the SG threshold curves occurred after the "1" write operation. Figure 2(a) shows these results, where the SG was a single Josephson junction. The I_W's indicate the write current levels for a "1" writing

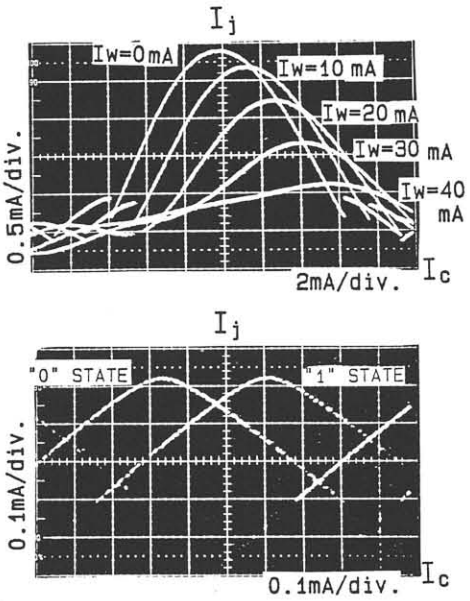

Fig. 2 Experimental threshold curves for typical sense gates after "1" writing on (a) previously reported vortex memory cell, and on (b) present memory cell.

operation. These curves were measured after decreasing the I_W to zero in order to avoid the influence of the write current.

Extracting only the shift effect is also necessary to achieve a wide sense operation margin. In our cell structure, this is realized as shown in Fig. 2(b), where the Josephson current, I_J, suppression was avoided. The curves were measured both after the "1" and "0" writing operations with large I_W levels. In these measurements, the SG was located outside of the VSR. The vortices were, therefore, prevented from entering the base electrode of the SG in order that Josephson current suppression not occur even after a "1" writing operation. This is made possible because I_J suppression results from the decrease in the effective Josephson junction area caused by the vortex normal cores entering the base electrode.

In addition to the above mentioned effect, the shift values of the SG threshold curves saturate when I_W becomes large in our cell structure. Figure 3 demonstrates this effect, which results from the saturation of the number of vortices stored in the VSR. On the other hand, shift values never saturate in the previously proposed cell structure.[4] This is because I_J becomes zero before the shift values saturate due to vortices entering the

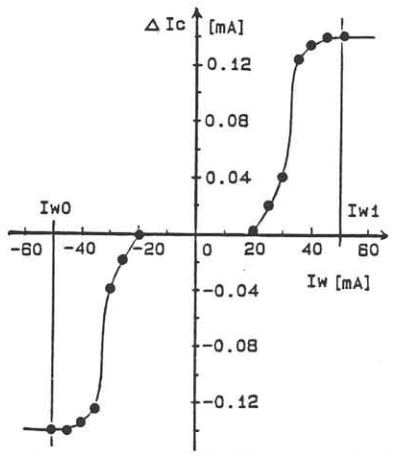

Fig. 3 Obtained threshold curve shifts(ΔI_C) as a function of write current(I_W) characteristics on memory cell. I_{W1} and I_{W0} indicate typical "1" and "0" write current levels, respectively.

base electrode of the sense junctions. This shift saturation effect is a considerable advantage from the viewpoint of improving the write operation margin as the write current level is set in the shift saturating region. Utilizing both the pure I_J shift effect and the shift saturation effect mentioned earlier, our memory cell can be operated stably in the 1,-1 mode.

4.Fabrication

The memory cell shown in Fig. 1 was fabricated by a conventional lead alloy process[5] with a 5-μm minimum line width. A Pb/In/Au film co-evaporated at a substrate temperature of 90 K[6] was used for the VSR film. The film thickness is 50nm. The VSR has an area of 5 x 8 μm^2. Figure 4 shows a SEM photograph of the fabricated memory cell, which occupies an area of 30 x 60 μm^2 or 72 minimum-linewidth squares. This cell is one-fourteenth the size of the conventional persistent current-type memory cell.[7]

The low-temperature co-evaporated film is used in the VSR to reduce the write current level. This is because a reduction in the write current level is expected with this co-evaporated film due to its small pinning force. In this type of memory cell, in which the SG cannot detect the vortices until they arrive near the SG, the write current level is determined by the pinning force rather than by

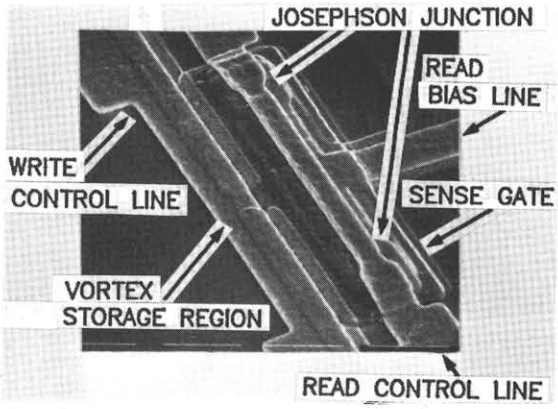

Fig. 4 SEM photograph of fabricated cell.

the low critical magnetic field,H_{c1}. As has been previously reported,[6] the grain size of the low-temperature co-evaporated film is smaller than that of the conventional sequentially deposited Pb/In/Au film evaporated at room temperature. A small pinning force is expected in the small-grain-sized film.

Utilizing this co-evaporated film, the write current level has been reduced to 7 - 50 mA. This value is one order of magnitude smaller than that for the previously reported vortex memory cell.[4]

5.Memory operation

Figure 5 shows a properly executed quasi-static test pattern, including NDRO, for full-and half-selected read conditions. The current labels are the same as those in Fig. 1. The sense signal, V_S, is the voltage across the SG. A positive pulse on I_W writes a "1", while a negative one corresponds to a "0" writing. A single pulse, I_B, simulates the read half-select conditions that would occur in a cell array. Coincident pulses, I_B and I_C, correspond to the read operation. After a "1"

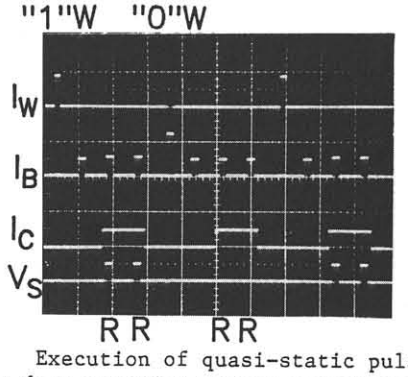

Fig. 5 Execution of quasi-static pulse test patterns demonstrating proper memory cell operation of cell in 1,-1 mode.

writing operation, voltage pulses corresponding to read pulses on I_B and I_C appeared on V_S. This indicates that a "1" writing and a "1" reading were operated properly. After a "0" writing, no pulse appeared on V_S, indicating that a "0" writing and a "0" reading were operated properly.

It is essential that the cell does not change its state during the read cycles or for these half-select conditions. In this quasi-static memory operation, it was confirmed that due to the shift saturation effect, the write operation margin became sufficiently wide. It was further proven that the memory operation margin was determined by the static SG margin. This relatively simple cell structure, containing only one or two Josephson junctions, makes the cell attractive in terms of memory chip fabrication.

6.Discussion

The reduction in the write current level was achieved by utilizing small pinning force films for the VSR. It is important to analyze this reduction mechanism. For this purpose, the saturated shift value of the SG threshold curves was measured with test cells whose distance from the vortex entrance edge of the VSR to the edge of the SG was varied. The data were plotted against the distance,L, as shown in Figure 6. It is clear that vortices accumulate near the entrance edge of the VSR. This means that the pinning force of the VSR film is still large;

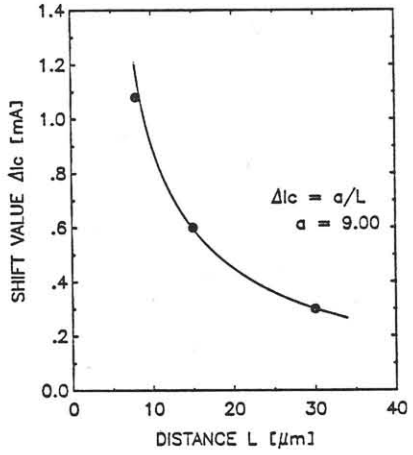

Fig. 6 Saturated shift value of SG threshold curves plotted against distance,L, from the vortex entrance edge of the VSR to the edge of the SG in the memory cell.

therefore, it is difficult for vortices to move toward the SG. This condition requires a large write current level for achiving a large shift value. It is clarified from this experiment that the farther reduction in the pinning force is still effective for reducing the write current level.

7.Conclusion

A new type of Abrikosov vortex memory cell has been studied, whose stable memory operation has been experimentally confirmed. This has been achieved by utilizing the shift-saturation effect and the 1,-1 mode operation. The write current level has been reduced one order of magnitude by using a Pb/In/Au film co-evaporated at a 90-K substrate temperature as the type II superconducting film of the VSR. In order to drive the cells by Josephson driver circuitry, this level should be reduced by at least one additional order of magnitude.

The cell occupies an area of 30 x 60 μm^2 with a 5-μm design rule. This is one-fourteenth of conventional cells. This small-sized memory cell is attractive as the basis for a high-density, high-speed cache memory.

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