

A Josephson Counter-Circuit with Two-Phase Power Supply

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This paper describes a new Josephson counter circuit which is driven with a two-phase power supply. The counter consists of a directly-coupled 4JL gate family (OR-, AND-, INVERT-, and amplifying-gate) to make a logic feed-back loop without any superconducting storage loop. A 3 μ m Nb/Al-oxide/Nb Josephson junction technology with a lead alloy wiring process developed were used in the circuit fabrication. In the counter circuit fabricated, counting, loading, and clearing operations have been successfully performed by feeding external control signals. Extensions to high speed operations and to 4 bit counter are discussed.

§1. Introduction

Recently, a remarkable progress has been seen in Josephson digital circuit technology. Several successful operations of Josephson circuits such as 8-bit adder, 4-bit multiplier, gate-array have been demonstrated¹⁻⁴). In these combinational logic circuits, a data-latch function is not employed. In the sequential logic circuit reported so far⁵), the latch function is based on a superconducting storage loop. The loop has large inductances to trap a few magnetic flux quanta. A new type of data-latch circuit, which has an advantage to reduce circuit size by excluding superconducting storage loop, has been already reported.⁶) This data-latch circuit consists of directly-coupled 4JL-gates driven by a two-phase monopolar power supply. By introducing this data-latch, we have composed a new Josephson counter circuit. A 3 μ m Nb/Al-oxide/Nb junction technology⁷) combined with a lead-alloy wiring process has been used to make the counter circuit.

§2. Counter-circuit design

A circuit block diagram of one-bit Josephson counter is shown in Fig.1. Two data-latch circuits (L1 and L2) and a

control circuit make a logic feed-back loop in the counter. The data-latch circuit, which consists of OR- and INVERT-gates, acts to hold an input-data state of "1" or "0" with the two-phase monopolar power supply (P1 and P2). L2 has dual-outputs of true (T) and complement (C) for dual-rail logic operations in the control circuit. The data for counting is stored in the form of a circulating propagation signal in the logic feed-back loop. Three operation modes to count numbers of the input signal state of \overline{S} , to load the external input state of \overline{DATA} (1/0), and to clear the state in the feed-back loop are selected by

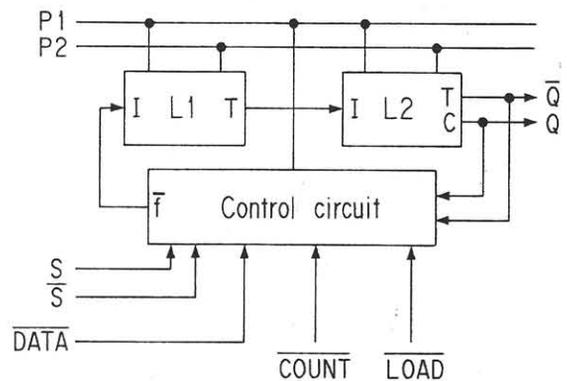


Fig.1 Block diagram of Josephson counter circuit.

Table I List of control commands for the Josephson counter.

Commands	$\overline{\text{COUNT}}$	$\overline{\text{LOAD}}$	S	\overline{S}	$\overline{\text{DATA}}$
Count	0	1	1/0	0/1	X
Load	1	0	X	X	0/1
Clear	1	1	X	X	X

feeding command signals at terminals of $\overline{\text{COUNT}}$ and $\overline{\text{LOAD}}$. Both the control function \overline{f}_n to perform these commands in the phase P1 and the counter output Q_{n+1} are given as follows.

$$\overline{f}_n = ((S_n + \overline{Q}_n)(\overline{S}_n + Q_n) + \overline{\text{COUNT}}_n)(\overline{\text{DATA}}_n + \overline{\text{LOAD}}_n), \quad (1)$$

$$Q_{n+1} = \overline{f}_n, \quad (2)$$

$$\text{and } \overline{Q}_{n+1} = \overline{f}_n, \quad (3)$$

where the integer n means the cycle time, and Q_{n+1} is the output obtained in the n+1th P1 phase. The control circuit is composed of two-stage 4JL OR-AND gates¹⁾, which are wired based on the above equations. Control commands for the counter are listed in Table I. Mark X in the table means that inputs are not in active.

The count mode is active with control signals of both $\overline{\text{COUNT}}$ of "0" and $\overline{\text{LOAD}}$ of "1" as shown in the table. At this mode, numbers of input signals S are counted. \overline{S} is required to hold the input state of the loop until the next input signal. Any input data of $\overline{\text{DATA}}$ do not affect the counting operation in this mode. The load command needs the control signals of both $\overline{\text{COUNT}}$ of "1" and $\overline{\text{LOAD}}$

of "0". At this mode, the $\overline{\text{DATA}}$ of "1" or "0" is loaded into the feed-back loop for any internal circuit conditions. The clear mode is used to reset the counting state by control signals of "1" of both $\overline{\text{COUNT}}$ and $\overline{\text{LOAD}}$. In this mode, no input signals are counted.

Figure 2 is a timing chart which shows the states in the counting operations. I(L1) and I(L2) are input signal states of L1 and L2, respectively. In the figure, the input signals of S come to the circuit at every active time durations of phase P1. Arrows mean the way how to circulate the signal state in the counter circuit. As is shown in the figure, let us suppose that the counter output Q is "0" at the first cycle time. A state "0" of I(L1) is caused by the coincidence function between the states of S="1" and Q="0". This data "0" is latched and transferred to L2 when the power P2 start to supply. Then, the state "0" of I(L2) is inverted and transferred back again to the output terminal, resulting to Q="1" at the next phase P1. These operations are repeated to count the input signals synchronizing to the two-phase power supply. Therefore, the counting operation can be performed.

Figure 3 shows a detail of the data-latch circuit L2, which generates dual outputs of true and compliment. Each output is designed to have a fanout of two using amplifying gates. Single junctions denoted by Jp and Jn in the figure are important to prevent racing

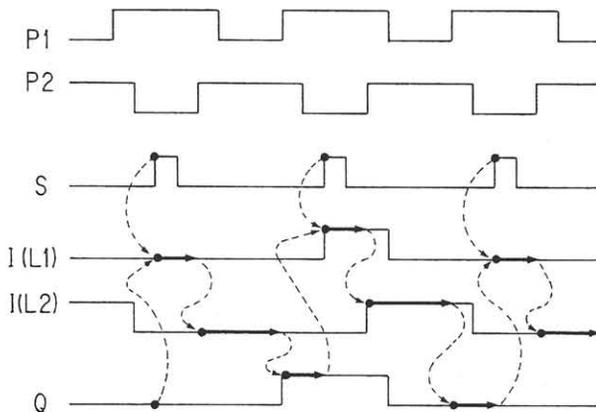


Fig.2 Timing chart of counting operations.

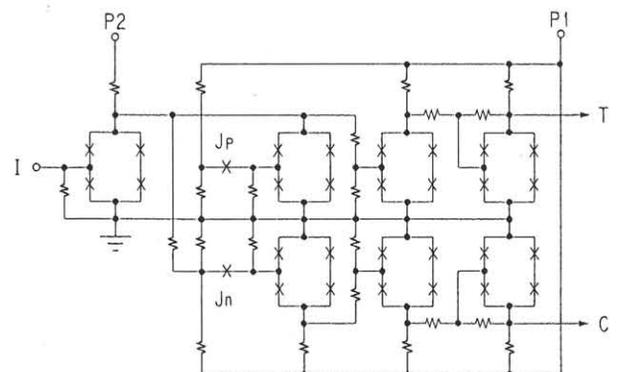


Fig.3 Latch circuit in Josephson counter.

actions of logic during the time duration of overlap of P1 and P2. In the L1 data-latch, the upper part of the latch circuit in Fig.3 was used to obtain single output of true(T).

The counter circuit was designed to operate by feeding the two-phase power into common power lines which are regulated at 11.2 mV with Josephson regulators. Circuit parameters were determined using a load resistance of $14\ \Omega$ and a 2.8 mV gap-voltage of the Nb/Al-oxide/Nb junction. In the circuit, OR gates were designed to have a maximum gate current of $200\ \mu\text{A}$ and a power dissipation of $1.7\ \mu\text{W}$.

§3. Fabrication

The counter circuit has been fabricated with a Nb/Al-oxide/Nb Josephson junction technology developed⁸⁾. A whole wafer junction-sandwich which has thicknesses of 200 nm and 150 nm of Nb films for base and counter electrodes, respectively, was made by DC magnetron sputtering. The tunnel barrier was made by a thermal oxidation of Al film surface with pure oxygen gas of 1 Torr at ambient temperature. Josephson critical current was controlled with an oxidation time. $560\ \text{A}/\text{cm}^2$ junctions were made to obtain a critical current of $50\ \mu\text{A}$ for each $3\ \mu\text{m}$ square junction. Each junction was defined by cut out from the sandwich with reactive

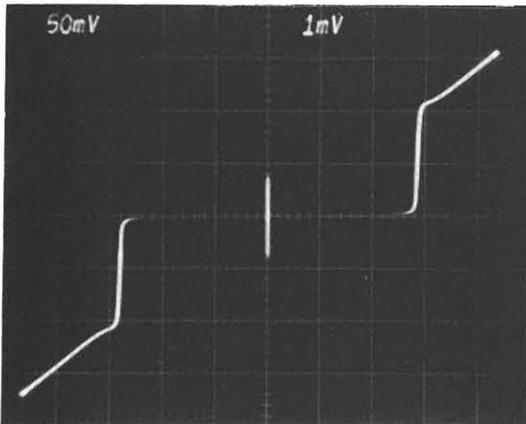


Fig.4 I-V curve of a $3\ \mu\text{m}$ Nb/Al-oxide/Nb junction. Vertical: $50\ \mu\text{A}/\text{div}$, Horizontal: $1\ \text{mA}/\text{div}$.

ion etching. Insulations between each junction were performed using a self-aligned SiO_2 ⁹⁾ evaporated film. Resistors were made of Au-In alloy film with a thickness of 30 nm to obtain a sheet resistance of $2\ \Omega/\square$. Inter-connections of the junctions and the resistors were performed by wiring with $3\ \mu\text{m}$ -line width Pb-In(10wt%) films using a lift-off technology. A typical I-V curve of the single $3\ \mu\text{m}$ Nb/Al-oxide/Nb junction fabricated for the counter circuit is shown in Fig.4. $V_m = 40\ \text{mV}$ and $V_{\text{gap}} = 2.85\ \text{mV}$ are observed in the curve. The 4JL gate array fabricated in a 100 series connection was found to have the variation of $\pm 13\%$ in the maximum gate current.

§4. Experimental results and discussion

Figure 5 shows a photograph of the counter-circuit fabricated using the $3\ \mu\text{m}$ Nb/Al-oxide/Nb junction technology. The circuit size of the counter is about $200 \times 330\ \mu\text{m}^2$. Experimental tests of the circuit were performed at a repetition rate of 6 KHz of the two-phase power supply. Signal currents of $75\ \mu\text{A}$ were fed into the input and control terminals. Figure 6 shows oscilloscope traces which indicate the operations for various patterns of count, load and clear. In the figure, the outputs for each command are observed one clock later after the time when the command is applied in the phase P1 as is explained in Fig.2. The

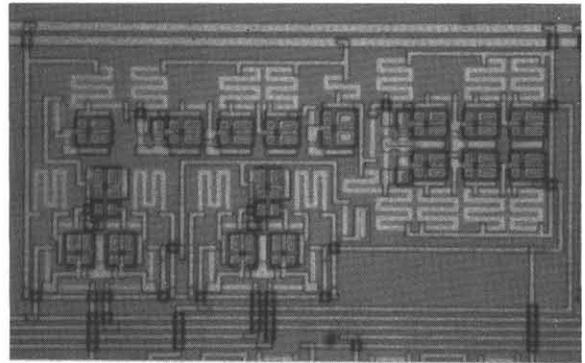


Fig.5 Photograph of Josephson counter circuit fabricated with $3\ \mu\text{m}$ Nb/Al-oxide/Nb junction technology.

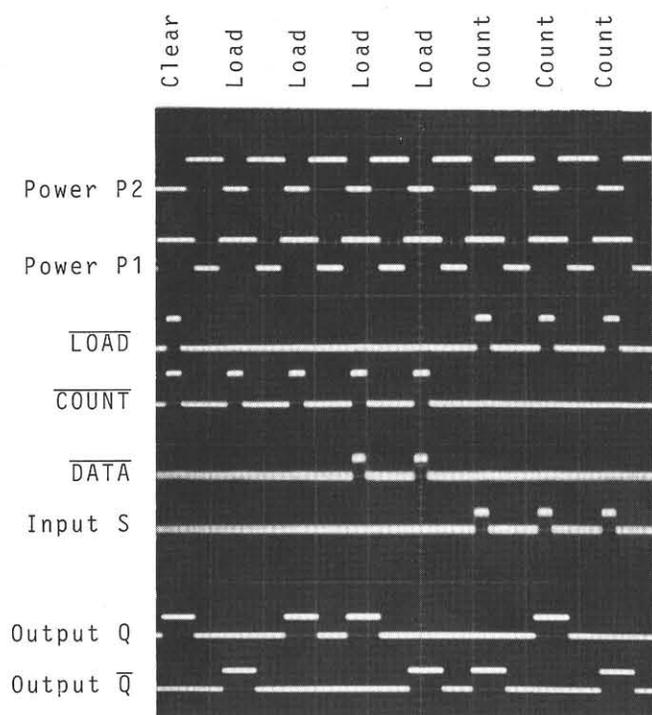


Fig.6 Full operations of the Josephson counter.

clear command is applied with both "1" of $\overline{\text{LOAD}}$ and $\overline{\text{COUNT}}$ into the circuit at the first phase P1. The outputs of $Q="0"$ and $Q="1"$ are observed in the next phase P1. For four times load commands are applied with input data of $\overline{\text{DATA}}="0"$, "0", "1", "1", sequentially. In the output traces of Q and \overline{Q} , it is found that the input data are correctly loaded into the counter. In the last three cycles, the counting operations are performed with three input signals. The last counting output is out of the figure.

Operating margins of $\pm 28\%$ and $\pm 35\%$ were measured in the dual-output data-latch circuit and the OR-AND gate, respectively. The margins for both these circuits designed are $\pm 35\%$. It should be noted that the low-frequency operations are not restricted by intrinsic delay time of the Josephson logic circuit. The nominal switching delay times of the OR gate and the OR-AND gate were evaluated to be 15 ps and 30 ps, respectively, by using computer simulations taking account of the parameters of the Nb/Al-oxide/Nb

junction⁷⁾. Based on these delay times, the counting time for each cycle is estimated to be 135 ps in the one-bit counter. A power dissipation is calculated to be 29 μW for the one-bit counter. A multi-bit counter can be designed by adding carry generation circuits to the series connected present counters. The carry generation circuit can be composed of an OR gate, an OR-AND gate and amplifying gates. For a 4-bit counter, the count operation time is expected to be 255 ps with a power dissipation of 170 μW .

§5. Conclusion

The Josephson counter which is driven by the two-phase power supply without the superconducting storage loop to store any magnetic flux quanta has been demonstrated. The circuit was fabricated using the 3 μm Nb/Al-oxide/Nb junction technology developed. The low-frequency tests for the counter functions of count, load, and clear were performed as expected.

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