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Novel Josephson Integrated Circuit Technology Based on Selective Trilayer Ion-Beam Etching Process

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A novel Josephson IC technology based on Nb/Nb-oxide/Pb-alloy tunnel junction formation by the selective trilayer ion-beam etching process (STIEP) has been developed. This technology uses Mo resistors patterned by RIE in SF_6 gas plasma. Pb-Au(4 wt.%)-In(12 wt.%) layers are used as counter electrodes and lines. Resistor-coupled Josephson logic (RCJL) gates using junctions with 2-μm minimum feature size have been fabricated using this technology. A standard deviation in the critical current of 250 series-connected OR gates is 3.5%. The shortest logic delay of the OR gate is 10 ps/gate.

1. Introduction

To date, various fabrication processes of Nb-based or NbN-based Josephson junctions have been developed [1-3]. Some of those junctions have also been integrated into Josephson IC's [4-5]. In order to increase the magnitude of integration, reduction in the junction size is required while maintaining the uniformity of the critical currents. We proposed a new Nb/Nb-oxide/Pb-alloy tunnel junction formation process which has the potential to achieve Josephson LSI's [6,7].

The process, which is called "selective trilayer ion-beam etching process" (STIEP), includes the following key steps: Nb/Nb-oxide/Pb-alloy trilayer formation involving in-situ thermal oxidation; junction area definition by deep UV lithography; highly selective Pb-alloy patterning by ion-beam etching (IBE); lift-off of an evaporated base electrode insulation layer. In the STIEP, high quality junction characteristics are easily obtained by Nb/Nb-oxide/Pb-alloy trilayer in-situ formation. The tunnel barrier formed by thermal oxidation has an advantage in the uniformity in the barrier thickness over oxide barriers formed by plasma oxidation and artificial barriers. The junction areas are patterned more accurately by IBE than by reactive ion etching (RIE), because of the anisotropic etching feature of the IBE.

We have developed a novel Josephson integrated circuit technology based on the STIEP. We have also fabricated resistor-coupled Josephson logic (RCJL) circuits [8] to evaluate the suitability of this technology for Josephson IC fabrication. In this paper, we describe the fabrication technology and the results of process evaluation.

2. IC Fabrication Process

Figure 1 shows a schematic cross-section of the RCJL circuit. The circuit fabrication steps are summarized in Table 1.

A Nb ground-plane layer is deposited and then patterned by RIE in CF_4. The ground-plane is insulated using an anodized Nb_2O_5 layer and an evaporated SiO layer.

A Mo resistor layer is deposited by rf sputtering and is patterned by RIE in SF_6. At 4.2 K, 170 nm thick films result in the sheet resistance of 1Ω/□. Figure 2 shows etch rates of Mo and SiO as a function of SF_6 gas pressure. The etch rate ratio of Mo to SiO is 5 at the pressure of 7 Pa. After RIE, Mo resistors are covered with SiO protection layers patterned by lift-off.

Contact holes to the ground-plane are opened in the ground-plane insulation layers by RIE in CF_4. The etch rate ratio of SiO to Nb is 4 at 5 Pa using a Teflon cathode. Prior to junction trilayer formation, the ground-plane is sputter cleaned in an rf Ar plasma in order to ensure superconducting contacts.

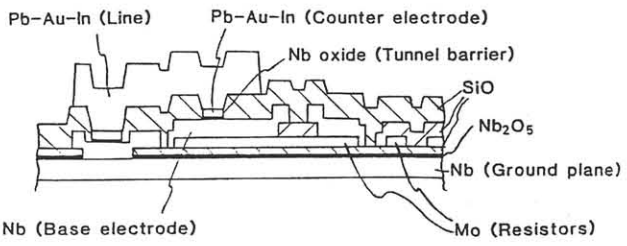


Fig.1. Schematic cross-section of the RCJL circuit.

Junctions are fabricated by the STIEP. A junction trilayer is sequentially formed over the substrate. A Nb base electrode layer is first deposited by rf sputtering. Next, the surface of the base electrode layer is thermally oxidized in O_2 atmosphere to form a tunnel barrier. Figure 3 shows the O_2 pressure dependence of junction critical currents. Pb-Au(4 wt.%)-In(12 wt.%) is selected as a counter electrode material, because of its chemical and mechanical stability. The counter electrode layer is formed by the sequential deposition of Pb, Au and In.

The trilayer is patterned by etching the top Pb alloy layer and the bottom Nb layer sequentially to form base electrodes and lines. The Pb alloy layer is etched by IBE. Then, the Nb oxide and Nb layers are etched by RIE in CF_4. At the pressure of 10 Pa, the etch rate ratio of Nb to SiO is 4.5.

Next, Josephson junction areas are defined by deep UV lithography, and etched by IBE. A positive photoresist (ODUR-1013) is used in the deep UV lithography. The etch rates of Pb alloy, Nb, Nb oxide and SiO are 120 nm/min, 14 nm/min, 27 nm/min and 37 nm/min, respectively. After IBE, the exposed surface of the base and counter electrodes are oxidized in O_2 plasma, followed by a SiO film deposition for base electrode insulation. The SiO film is patterned by lift-off using the same photoresist mask that defined the junction area earlier.

Finally, a Pb-Au(4 wt.%)-In(12 wt.%) layer for interconnecting lines is deposited and then patterned by IBE.

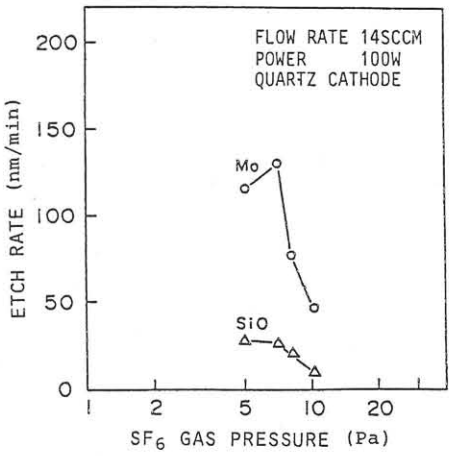


Fig.2. Etch rates of Mo and SiO as a function of SF_6 gas pressure.

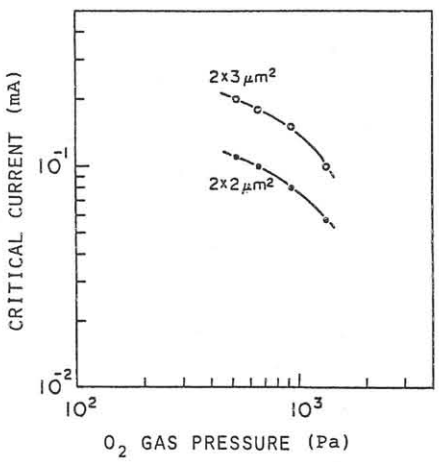


Fig.3. O_2 pressure dependence of junction critical currents. Thermal oxidation time is 30 minutes.

Table 1. Circuit fabrication process.

	Process	Material	Thickness	Method
1.	Ground-plane formation	Nb	350nm	Sputter deposition, RIE in CF_4
2.	Ground-plane insulation	Nb_2O_5	35nm	Anodization
		SiO	100nm	Evaporation
3.	Resistor formation	Mo	170nm	Sputter deposition, RIE in SF_6
4.	Resistor protection	SiO	200nm	Evaporation, Lift-off
5.	Contact hole formation	-	-	RIE in CF_4
6.	Junction trilayer formation	Nb	250nm	Sputter deposition
		Nb oxide	-	Thermal oxidation
		Pb alloy	150nm	Evaporation
7.	Base electrode etching	Pb alloy	-	IBE (Ar)
		Nb	-	RIE in CF_4
8.	Junction definition	Pb alloy	-	Deep UV lithography, IBE (Ar)
9.	Base electrode insulation	SiO	350nm	Evaporation, Lift-off
10.	Line formation	Pb alloy	600nm	Evaporation, IBE (Ar)

* The STIEP consists of the steps 6-9.

Throughout the process, only the low temperature procedures are used after the trilayer formation. The highest process temperature is 90°C for ODUR-1013 prebaking. It was found that the process temperature less than 100°C does not affect on the junction characteristics.

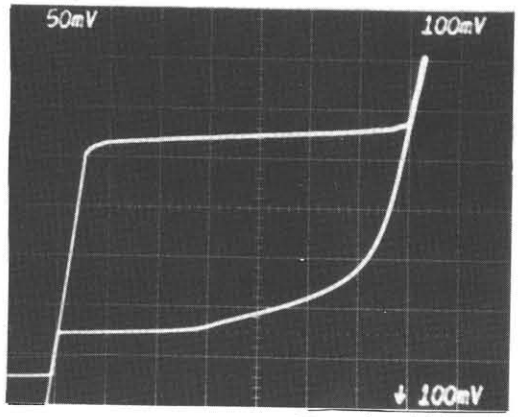
3. Process Evaluation

The uniformity of junction critical currents was measured using arrays of 250 series-connected junctions with dimensions of 2×3 μm^2, 2×2.5 μm^2 and 2×2 μm^2. The mean value of the critical currents are 200 μA, 160 μA and 115 μA, respectively. The barrier is formed by thermal oxidation at 530 Pa in O_2 for 30 minutes. The standard deviation in the critical currents of 250 junctions is less than 4% for 2×3μm^2 junctions. The maximum deviation in the mean critical current of each array is ±6% in the area of 25×25 mm^2.

The uniformity of critical gate currents was measured using arrays of 250 series-connected RCJL OR gates layouted in the area of 600×760 μm^2. Each gate contains one 2×2.5μm^2 and two 2×3 μm^2 junctions. Current-voltage characteristics of the 250 series-connected OR gates are shown in Fig. 4. A standard deviation in the critical gate current was 3.5% The maximum deviation in the mean critical current of each array is ±6% in the area of 25×25 mm^2.

The resistance of the 170 nm thick resistors with line widths of 2μm and 5μm are measured. The resistance ratios of these resistors correspond to their geometrical ratios correctly. The maximum deviation in the resistance for each resistor with different dimension is less than 5.5% in the area of 25×25 mm^2.

The RCJL OR gate, AND gate and 2/3-MAJORITY gate were fabricated. The AND and 2/3-MAJORITY gates use 2×2μm^2 junctions. The minimum line widths of resistors and interconnecting lines are 2μm and 3μm, respectively. The minimum pattern gap of electrodes and the minimum alignment margin are 1 μm. The OR gate size is 40×30 μm^2 excluding a dropping resistor area. The gate sizes of AND and 2/3-MAJORITY gates are 40×30 μm^2 and 40×40



X-axis:100mV/div.
Y-axis:0.1mA/div.

Fig.4. Current-voltage characteristics of an array of 250-series-connected RCJL OR gates.

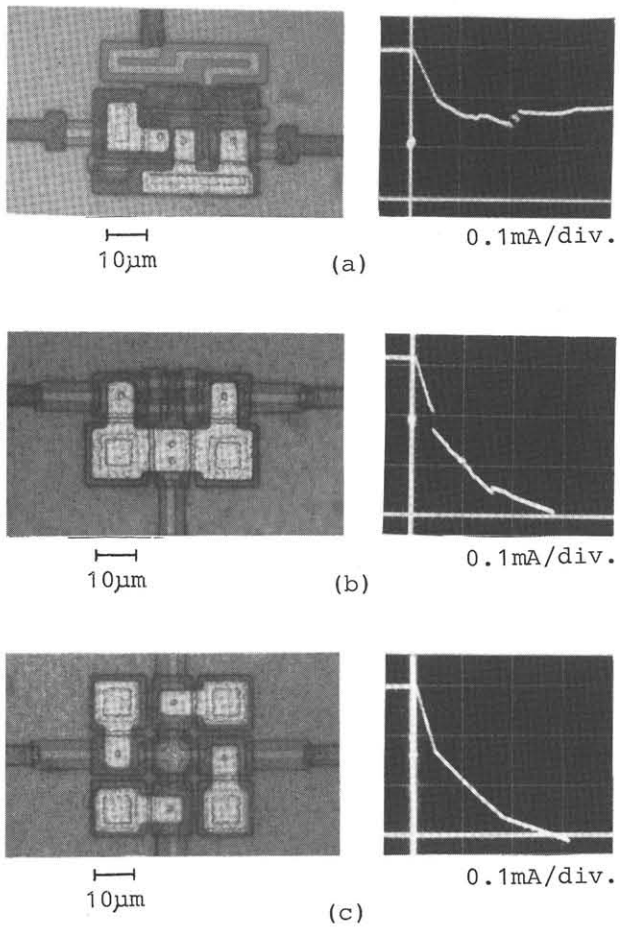


Fig.5. Photomicrographs and measured threshold curves of (a)the OR gate, (b)the AND gate and (c) the 2/3-MAJORITY gate.

μm^2, respectively. Figure 5 shows photographs and measured threshold curves of (a) the OR gate, (b) the AND gate and (c) the 2/3-MAJORITY gate. The observed threshold curves agree with the theoretical ones [8].

The logic delay of the RCJL OR gate was measured across a cascade chain [9] of 10 gates. An equivalent circuit of the OR gate is shown in Fig. 6 (a). The shortest logic delay of 10 ps/gate was obtained as shown in Fig. 6 (b). The power dissipated at a dropping resistor was measured to be 4.7 μW.

4. Conclusion

A novel Josephson IC technology based on Nb/Nb-oxide/Pb-alloy tunnel junction formation by the selective trilayer ion-beam etching process (STIEP) has been developed. A Mo layer patterned by RIE in SF_6 is used as resistors. Pb-Au(4 wt.%)-In(12 wt.%) layers are used as counter electrodes and lines. Resistor-coupled Josephson logic (RCJL) gates using junctions with 2-μm minimum feature size have been fabricated using this technology. The suitability of this technology for Josephson LSI fabrication is demonstrated.

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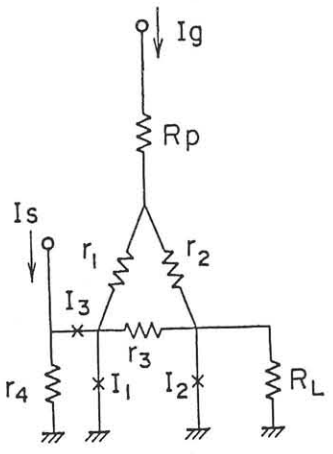
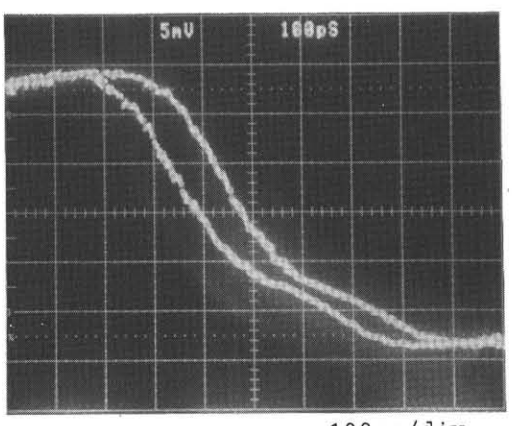


$I_1=I_2=0.15mA, I_3=0.12mA,$

$r_1=r_2=r_3=r_4=0.87\Omega, R_L=6.5\Omega, R_P=50\Omega$

(a)



100ps/div.

(b)

Fig.6. (a) The equivalent circuit of the RCJL OR gate,and (b) logic delay measurement for the 10 OR gates. Waveforms are inverted by a wide band linear amplifier.