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TDDB Measurements of SiO_2 Gate and $SiO_2/Si_3N_4/SiO_2$ Gate Structure

J.Mitsuhashi, K.Sugimoto, M.Hirayama, S.Sadahiro and T.Matsukawa

LSI R&D Lab. Mitsubishi Electric Corporation

4-1 Mizuhara, Itami, Hyogo 664 Japan

$SiO_2/Si_3N_4/SiO_2$ stacked gates and SiO_2 gates are investigated using TDDB measurements. Top SiO_2 layer reduces an electron trapping in the stacked gate and improves intrinsic breakdown properties. The intrinsic breakdown properties of the stacked gate are determined by the SiO_2 layer. And, Si_3N_4 layers have reduced random failure of TDDB characteristics which occurs by the weak spots dotted homogeneously following Poisson's distribution in bottom SiO_2 layers. This stacked structure gate is considered to be very efficient to obtain high reliable gates for VLSIs.

§1. Introduction

One of the important problems in Dynamic RAMs and EEPROMs is the reduction of reliability of thin gate insulators due to increased electric fields by scaling down. As the gate insulators have become thinner, pin hole density is also increasing.[1] In these situations, an application of Si_3N_4 with high dielectric constant can be considered for the gate insulator. As a most promising structure for these devices, SiO_2 (top)/Si_3N_4/SiO_2 (bottom) stacked gate structure has been studied. [2,3] There are few reports, however, on the reliability of this structure.[4]

This paper describes the reliability aspects of the $SiO_2/Si_3N_4/SiO_2$ stacked gate and SiO_2 gate under high electric stress fields using TDDB(Time-Dependent Dielectric Breakdown) measurement.

§2. Specimen and Experimental Techniques

The devices measured were MIS capacitors fabricated on (100) p- or n-type C-Z Si-substrate with impurity concentrations of $2\text{-}6\times10^{15}$ atoms/cm^3. The gate oxide layers , 7.0-17.7 nm thick, were thermally grown in dry O_2/HCl at 900 °C. Si_3N_4 films were deposited on the oxides by LPCVD to fabricate the stacked gate. The surfaces of Si_3N_4 layers were oxidized at 900 °C in dry O_2 ambient. Thicknesses of these stacked gates were 1.5/9.9-16/7-17.7 nm. The MIS capacitor areas were 0.12-0.98 mm^2. The oxide-equivalent gate thickness(T_g) is defined by $T_g=(T_{oxt}+ T_{sin} \times \varepsilon_{sio}/\varepsilon_{sin} +T_{oxb})$, where T_{oxt}, T_{sin} and T_{oxb} are the thickness of the top oxide, nitride and bottom oxide,and ε_{sio} and ε_{sin} represent the dielectric constant of SiO_2 and Si_3N_4, respectively. TDDB characteristics were measured by applying the constant voltage to the MIS capacitors. The voltage was applied to get the accumulation mode of capacitors, and electric stress field (E_g) through the gate insulator was calculated using T_g and capacitance measured in accumulation mode. The flat band voltage shift (ΔV_{FB}) was also measured by C-V mater of 100 KHz. Time-zero dielectric breakdown characteristics were investigated by applying step voltage increasing with a constant rate.

§3. Results

The TDDB measurement is one of the most suitable methods for evaluating the dielectric layers, because this measurement can directly estimate its reliability.

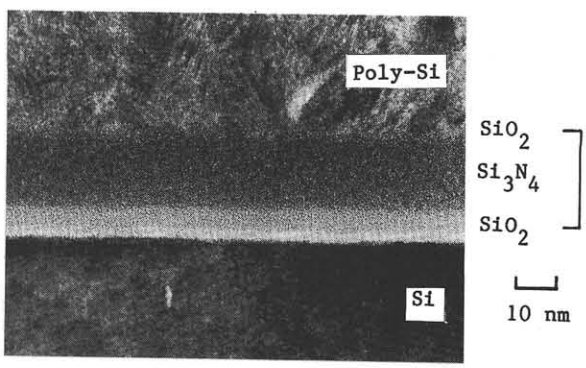

Fig.1 Cross-sectional micrograph of the $SiO_2/Si_3N_4/SiO_2$ stacked gate.

A cross-sectional TEM microphotograph of the $SiO_2/Si_3N_4/SiO_2$ gate is shown in Fig.1. From this photograph, thickness of each layer can be measured and it is found that the asperity of Si_3N_4 layer is reduced to ±1.5 nm by re-oxidation process.

3-1. Gate Current

Fig.2 shows the I-E characteristics of the stacked gate and SiO_2 gate. Solid lines and broken lines represent the results of the stacked gate and SiO_2 gate, respectively. This I-E characteristics of the stacked gate depend upon a

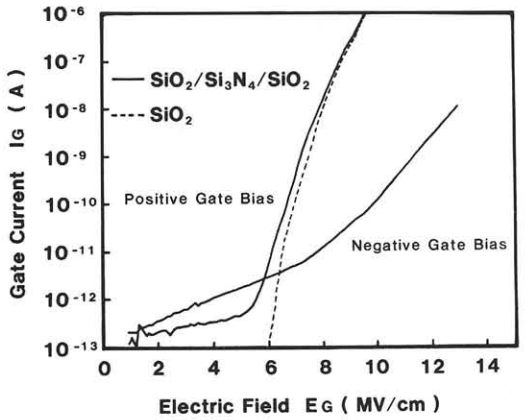

Fig.2 Gate current and Electric field characteristics. The current under positive gate bias follows F-N mechanism and that under negative bias follows P-F mechanism.

polarity of gate bias. In the case of positive gate bias, the curve is almost consist with that of the SiO_2 gate. But for the negative bias, the curve shows less dependence upon the electric field. Thus the gate current under the negative gate bias is much less than that under the positive bias for even the same electric field over about 5 MV/cm. Judging from Fowler-Nordheim (F-N) plot and Pool-Frenkel (P-F) plot of both curves, conduction mechanism through the stacked gate is F-N current under the positive gate bias and P-F current under the negative gate bias.

3-2. TDDB Characteristics

The TDDB characteristics are shown in Fig.3 for three types of the gate structure under E_g of -9 MV/cm using p-type substrate. The broken line represents a result of the SiO_2 gate and solid line is that of the stacked gate. Median Time to

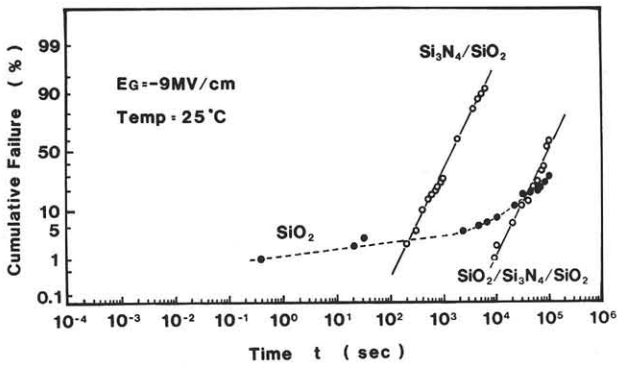

Fig.3 TDDB characteristics of the SiO_2 gate (16 nm), Si_3N_4/SiO_2 gate and $SiO_2/Si_3N_4/SiO_2$ stacked gate (1.5/11/9.4 nm). (p-type sub)

Failure (MTF) for the SiO_2 gate is longer than 10^5 sec. On the other hand, MTF value for the Si_3N_4/SiO_2 double layer gate is about 10^3 sec. But, by re-oxidizing this gate structure, MTF value becomes about two order of magnitude longer and is almost the same as that of the SiO_2 gate. TDDB data at the higher temperature show this tendency more clearly. Therefore, the intrinsic breakdown phenomenon of the stacked gate capacitor is found to be determined by the SiO_2 gate layer. Also, it must be noted that the stacked gate has no random failure until its intrinsic breakdown.

An activation energy (ΔE_a) of this breakdown phenomenon is measured as ΔE_a=0.38 eV for the SiO_2 gate and 0.31 eV for the stacked gate. Both values are almost the same, and it predicts that the intrinsic breakdown of the stacked gate occurs through the same mechanism as that of the SiO_2

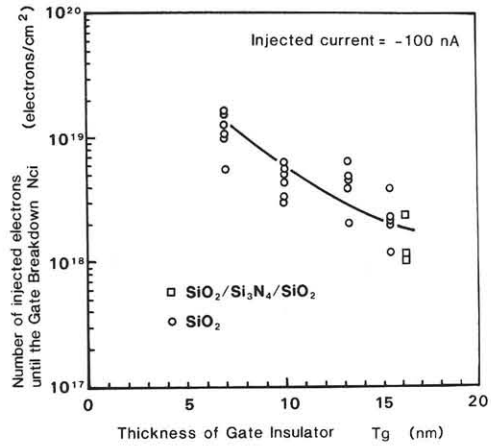

Fig.4 Gate insulator thickness dependence of the critical number of injected electrons which cause the intrinsic breakdown.

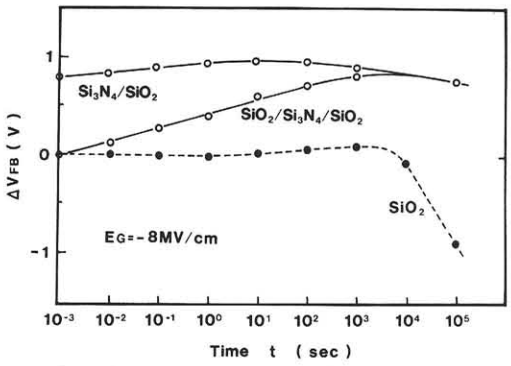

Fig.5 Relationship between ΔV_{FB} and the aging time. The thickness of SiO_2 and stacked gates are 17.7 nm and (1.5/)11/17.7 nm.

gate. The intrinsic breakdown occurs when the number of injected electrons reaches the critical value (N_c). This N_c value depends upon the thickness of gate layer T_g as shown in Fig.4. The value of N_c increases with decreasing T_g. This is considered to be concerned with the electron trapping in the gate layer.[6)]

The relationship between ΔV_{FB} and the aging time is shown in Fig.5 for three types of the gate structure on the p-type substrate. Under this aging stress condition of E_g=-8 MV/cm, the SiO_2 gate shows no remarkable V_{FB} shift until 10^3sec. The stacked gate shows a positive V_{FB} shift and the trapping efficiency of electrons is different among two structures of stacked gates. The top SiO_2 layer is efficient for reducing the electron trapping at the interface between the bottom SiO_2 and Si_3N_4 layer. The results for the MIS capacitor on n-type substrate are similar to those obtained for p-type substrate. The V_{FB} shift is negative and very small under $|E_g|$ of 5 MV/cm.

3-3. Random Failure Characteristics

As shown in Fig.3, the SiO_2 gate shows random failure until it reaches the intrinsic breakdown. This failure is seemed to be caused by the weak spots in the SiO_2 layer, considering a capacitor area dependence of the failure rate. Fig.6 shows a Weibull plot of a random failure for the SiO_2 gate under relatively low E_g of 7 MV/cm. The cumulative failure increases following Weibull distribution for each samples with three different gate area (S_g). Fig.7 clears a gate area dependence of the cumulative failure in terms of Weibull parameter t_o. A linear line on this figure shows that these data points satisfy the following equations,

$$F(t)=1-\exp(-t^{0.18}/t_0)$$
$$=1-\exp(-a(t)\times S_g)$$

,where F(t) is cumulative failure rate, and a(t) denots the surface density of the weak spots. Then, the weak spots in the SiO_2 layer are considered to be distributed homogeneously following Poisson's distribution.

3-4. Effects of Si_3N_4 Layer for TDDB

The TDDB characteristics of the stacked gate and Si_3N_4 gate on the n-type substrate under E_g of 9 MV/cm is shown in Fig.8. Although the MTF value of intrinsic breakdown becomes shorter than that shown in Fig.3 because of applying the positive

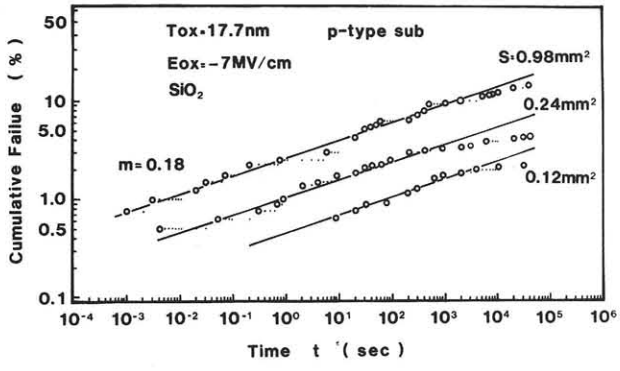

Fig.6 Weibull plot of TDDB data for the SiO_2 gate (17.7 nm) under the low stress field of 7 MV/cm. The gate area S_g is a parameter.

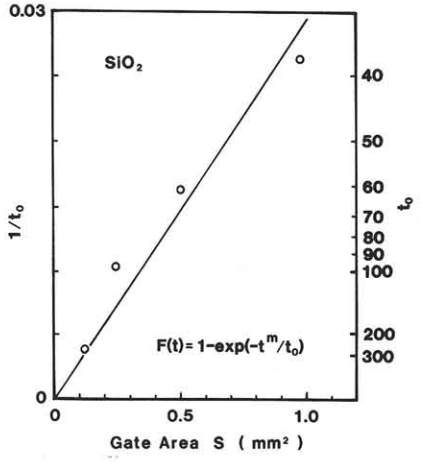

Fig.7 Relationship between Weibull parameter t_0 and the gate area S_g which is calculated from the data in Fig.6.

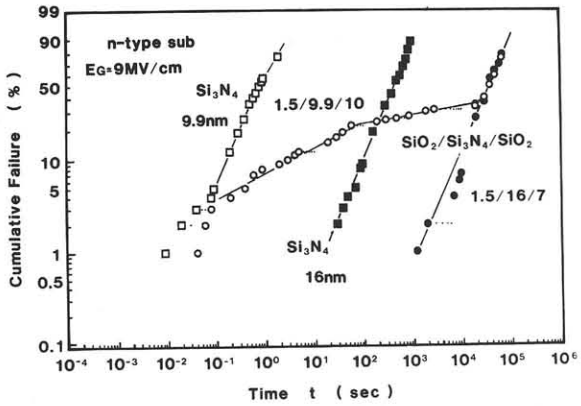

Fig.8 TDDB characteristics of the Si_3N_4 gate and $SiO_2/Si_3N_4/SiO_2$ stacked gate with the different thickness of Si_3N_4 layer. (n-type sub)

gate bias, the same characteristics as those of p-type substrate is shown here. In this case, the different results are obtained in regard to the thickness ratio of Si_3N_4/SiO_2. The sample with the ratio of 16/7 nm (filled circles in the figure) shows no random failure in this experiment, while the sample of 9.9/10 nm (open circles) shows random failure like the SiO_2 gate. The TDDB characteristics of Si_3N_4 layer with the thickness of 9.9 and 16 nm are shown in the same figure. For the 16 nm-thickness layer, MTF value of $5x10^2$ sec is obtained, but for the 9.9 nm thickness, MTF value becomes about three orders of magnitude shorter. This result shows that the weak spots in the SiO_2 layer are covered by Si_3N_4 layer. This covering effect was more remarkable at higher temperatures.

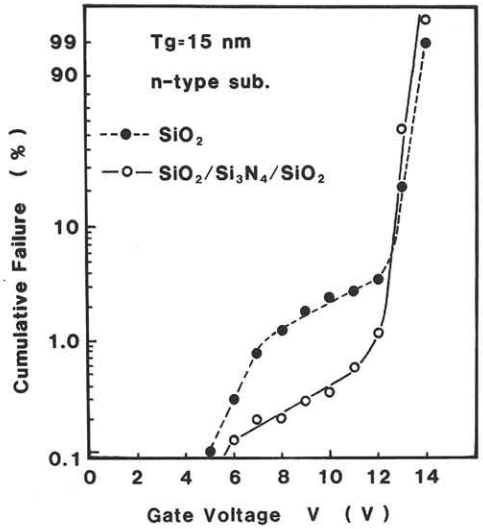

Fig.9 Time-zero dielectric breakdown characteristics of the SiO_2 and $SiO_2/Si_3N_4/SiO_2$ stacked gate.

Time-zero dielectric breakdown characteristics are shown in Fig.9 for the stacked gate (1.5/10/10 nm) and the SiO_2 gate (16 nm) on the n-type substrate. Both curves show the same intrinsic breakdown voltage. For lower voltage than this, cumulative failure is proportional to the electric field and the stacked gate shows lower failure rate than the SiO_2 gate. These correspond with the results of TDDB measurement mentioned above.

§4. Summary

The $SiO_2/Si_3N_4/SiO_2$ stacked gate and SiO_2 gate are investigated using TDDB measurements. The stacked gate has two different conduction mechanisms according to the gate bias polarity. For both conduction, the Si_3N_4 layer prevent the random failure of TDDB characteristics from occurring. The top re-oxidized SiO_2 layer improves the intrinsic breakdown properties by reducing the electron trapping at the interface between Si_3N_4 and SiO_2 layer. The intrinsic breakdown properties are, however, determined by the SiO_2 layer.

Therefore, this stacked gate structure is considered to be efficient to obtain high reliable gates.

§5. Acknowledgments

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§6. References

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