TDDB Measurements of SiO$_2$ Gate and SiO$_2$/Si$_3$N$_4$/SiO$_2$ Gate Structure

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SiO$_2$/Si$_3$N$_4$/SiO$_2$ stacked gates and SiO$_2$ gates are investigated using TDDB measurements. Top SiO$_2$ layer reduces an electron trapping in the stacked gate and improves intrinsic breakdown properties. The intrinsic breakdown properties of the stacked gate are determined by the SiO$_2$ layer. And, Si$_3$N$_4$ layers have reduced random failure of TDDB characteristics which occurs by the weak spots dotted homogeneously following Poisson's distribution in bottom SiO$_2$ layers. This stacked structure gate is considered to be very efficient to obtain high-reliable gates for VLSIs.

§1. Introduction

One of the important problems in Dynamic RAMs and ERPROMs is the reduction of reliability of thin gate insulators due to increased electric fields by scaling down. As the gate insulators have become thinner, pin hole density is also increasing. In these situations, an application of Si$_3$N$_4$ with high dielectric constant can be considered for the gate insulator. As a most promising structure for these devices, SiO$_2$ (top)/Si$_3$N$_4$/SiO$_2$ (bottom) stacked gate structure has been studied. There are few reports, however, on the reliability of this structure.

This paper describes the reliability aspects of the SiO$_2$/Si$_3$N$_4$/SiO$_2$ stacked gate and SiO$_2$ gate under high electric stress fields using TDDB (Time-Dependent Dielectric Breakdown) measurement.

§2. Specimen and Experimental Techniques

The devices measured were MIS capacitors fabricated on (100) p- or n-type C-Z Si-substrate with impurity concentrations of 2-6x10$^{15}$ atoms/cm$^3$. The gate oxide layers, 7.0-17.7 nm thick, were thermally grown in dry O$_2$/HCl at 900°C. Si$_3$N$_4$ films were deposited on the oxides by LPCVD to fabricate the stacked gate. The surfaces of Si$_3$N$_4$ layers were oxidized at 900°C in dry O$_2$ ambient. Thicknesses of these stacked gates were 1.5/9.9-16/7-17.7 nm. The MIS capacitor areas were 0.12-0.98 mm$^2$. The oxide-equivalent gate thickness ($T_X$) is defined by $T_X = (T_{oxt} + T_{sin} + \varepsilon_{SiO_2}/\varepsilon_{SiO_2} + T_{oxb})$, where $T_{oxt}$, $T_{sin}$, and $T_{oxb}$ are the thickness of the top oxide, nitride and bottom oxide, and $\varepsilon_{SiO_2}$ and $\varepsilon_{SiO_2}$ represent the dielectric constant of SiO$_2$ and Si$_3$N$_4$, respectively. TDDB characteristics were measured by applying the constant voltage to the MIS capacitors. The voltage was applied to get the accumulation mode of capacitors, and electric stress field ($E_S$) through the gate insulator was calculated using $T_S$ and capacitance measured in accumulation mode. The flat band voltage shift ($\Delta V_{FB}$) was also measured by C-V meter of 100 KHz. Time-zero dielectric breakdown characteristics were investigated by applying step voltage increasing with a constant rate.

§3. Results

The TDDB measurement is one of the most suitable methods for evaluating the dielectric layers, because this measurement can directly estimate its reliability.

Fig.1 Cross-sectional micrograph of the SiO$_2$/Si$_3$N$_4$/SiO$_2$ stacked gate.
A cross-sectional TEM microphotograph of the SiO$_2$/Si$_3$N$_4$/SiO$_2$ gate is shown in Fig.1. From this photograph, thickness of each layer can be measured and it is found that the asperity of Si$_3$N$_4$ layer is reduced to ±1.5 nm by re-oxidation process.

3-1. Gate Current

Fig.2 shows the I-E characteristics of the stacked gate and SiO$_2$ gate. Solid lines and broken lines represent the results of the stacked gate and SiO$_2$ gate, respectively. This I-E characteristics of the stacked gate depend upon a polarity of gate bias. In the case of positive gate bias, the curve is almost consist with that of the SiO$_2$ gate. But for the negative bias, the curve shows less dependence upon the electric field. Thus the gate current under the negative gate bias is much less than that under the positive bias for even the same electric field over about 5 MV/cm. Judging from Fowler-Nordheim (F-N) plot and Poole-Frenkel (P-F) plot of both curves, conduction mechanism through the stacked gate is F-N current under the positive gate bias and P-F current under the negative gate bias.

3-2. TDDB Characteristics

The TDDB characteristics are shown in Fig.3 for three types of the gate structure under $E_o$ of $-9$ MV/cm using p-type substrate. The broken line represents a result of the SiO$_2$ gate and solid line is that of the stacked gate. Median Time to Failure (MTF) for the SiO$_2$ gate is longer than $10^5$ sec. On the other hand, MTF value for the Si$_3$N$_4$/SiO$_2$ double layer gate is about $10^3$ sec. But, by re-oxidizing this gate structure, MTF value becomes about two order of magnitude longer and is almost the same as that of the SiO$_2$ gate. TDDB data at the higher temperature show this tendency more clearly. Therefore, the intrinsic breakdown phenomenon of the stacked gate capacitor is found to be determined by the SiO$_2$ gate layer. Also, it must be noted that the stacked gate has no random failure until its intrinsic breakdown.

An activation energy $(\Delta E_a)$ of this breakdown phenomenon is measured as $\Delta E_a = 0.38$ eV for the SiO$_2$ gate and 0.31 eV for the stacked gate. Both values are almost the same, and it predicts that the intrinsic breakdown of the stacked gate occurs through the same mechanism as that of the SiO$_2$ gate.

Fig.4 Gate insulator thickness dependence of the critical number of injected electrons which cause the intrinsic breakdown.
The aging stress condition of capacitor SiO₂ among the structure value (N.). This Nc value is considered to be concerned with the electron trapping in the gate layer.6)

The relationship between ΔVFB and the aging time is shown in Fig.5 for three types of the gate structure on the p-type substrate. Under this aging stress condition of Eg=8 MV/cm, the SiO₂ gate shows no remarkable VFB shift until 10³ sec. The stacked gate shows a positive VFB shift and the trapping efficiency of electrons is different among two structures of stacked gates. The top SiO₂ layer is efficient for reducing the electron trapping at the interface between the bottom SiO₂ and Si₃N₄ layer. The results for the MIS capacitor on n-type substrate are similar to those obtained for p-type substrate. The VFB shift is negative and very small under |Eg| of 5 MV/cm.

3-3. Random Failure Characteristics

As shown in Fig.3, the SiO₂ gate shows random failure until it reaches the intrinsic breakdown. This failure is seemed to be caused by the weak spots in the SiO₂ layer, considering a capacitor area dependence of the failure rate. Fig.6 shows a Weibull plot of a random failure for the SiO₂ gate under relatively low Eg of 7 MV/cm. The cumulative failure increases following Weibull distribution for each samples with three different gate area (S₀). Fig.7 shows a gate area dependence of the cumulative failure in terms of Weibull parameter t₀. A linear line on this figure shows that these data points satisfy the following equations,

\[ F(t) = 1 - \exp(-t/t_0) \]

where F(t) is cumulative failure rate, and a(t) denotes the surface density of the weak spots. Then, the weak spots in the SiO₂ layer are considered to be distributed homogeneously following Poisson’s distribution.

3-4. Effects of Si₃N₄ Layer for TDDB

The TDDB characteristics of the stacked gate and Si₃N₄ gate on the n-type substrate under Eg of 9 MV/cm is shown in Fig.8. Although the MTF value of intrinsic breakdown becomes shorter than that shown in Fig.3 because of applying the positive
gate bias, the same characteristics as those of p-type substrate is shown here. In this case, the different results are obtained in regard to the thickness ratio of $\text{Si}_3\text{N}_4/\text{SiO}_2$. The sample with the ratio of 16/7 nm (filled circles in the figure) shows no random failure in this experiment, while the sample of 9.9/10 nm (open circles) shows random failure like the $\text{SiO}_2$ gate. The TDDB characteristics of $\text{Si}_3\text{N}_4$ layer with the thickness of 9.9 and 16 nm are shown in the same figure. For the 16 nm-thickness layer, MTF value of $5\times10^2$ sec is obtained, but for the 9.9 nm thickness, MTF value becomes about three orders of magnitude shorter. This result shows that the weak spots in the $\text{SiO}_2$ layer are covered by $\text{Si}_3\text{N}_4$ layer. This covering effect was more remarkable at higher temperatures.

Time-zero dielectric breakdown characteristics are shown in Fig.9 for the stacked gate (1.5/10/10 nm) and the $\text{SiO}_2$ gate (16 nm) on the n-type substrate. Both curves show the same intrinsic breakdown voltage. For lower voltage than this, cumulative failure is proportional to the electric field and the stacked gate shows lower failure rate than the $\text{SiO}_2$ gate. These correspond with the results of TDDB measurement mentioned above.

§4. Summary

The $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate and $\text{SiO}_2$ gate are investigated using TDDB measurements.

The stacked gate has two different conduction mechanisms according to the gate bias polarity. For both conduction, the $\text{Si}_3\text{N}_4$ layer prevent the random failure of TDDB characteristics from occurring. The top re-oxidized $\text{SiO}_2$ layer improves the intrinsic breakdown properties by reducing the electron trapping at the interface between $\text{Si}_3\text{N}_4$ and $\text{SiO}_2$ layer. The intrinsic breakdown properties are, however, determined by the $\text{SiO}_2$ layer.

Therefore, this stacked gate structure is considered to be efficient to obtain high reliable gates.

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§6. References