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XMOS Transistor for a 3D-IC

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In three dimensional integrated circuits, device characteristics of an MOS transistor in one active layer can be affected by electrical interference from active elements or wirings in underlying active layer. This will cause less design freedom of device layout for the upper active layer and be a problem to realize 3D-IC's. To solve this problem, we have proposed an XMOS transistor structure having an additional bottom gate which acts with the upper gate as a shield of its channel region from such electrical interference. Also, we reported that its symmetrical structure as shown in Fig. 1 could be suitable for reducing the so-called short channel effect[1]. In this report, it is shown by more detail finite element numerical analysis that the subthreshold characteristics is improved with thin active layer and the current flowing through the upper surface channel is controlled widely not only by the potential of the upper gate but by that of the bottom gate. Moreover, it is shown that the threshold voltage shift seen from the upper gate by the potential of the bottom gate and vice versa is observed in experimentally fabricated devices.

Fig. 2 shows the calculated subthreshold characteristics of XMOS transistors for two different values of the active silicon layer thickness, Tsi and for three different values of channel length, L for each Tsi. Upper and bottom gate bias voltages, Vgu and Vgl are taken equal. When Tsi is 300 nm, the slope dVgu/d(logIds) is about 80 mV/decade and which is almost independent on channel length down to 0.6 μm. When Tsi is made thinner, the slope is improved to about 60 mV/decade which is nearly equal to theoretical limit of 2.3(kT/q)/decade. Also, smaller curve shift by reducing channel length is shown.

Fig. 3 shows similar characteristics of Fig. 2 though the bottom gate bias voltage, Vgl is fixed and it is taken as a parameter. When Vgl is 0.0 V, the upper channel current is dominant component of drain current except at low Vgu. In low Vgu case, the bottom channel current shown by broken line becomes dominant component instead. This tendency is also seen when Vgl is -0.5 V however the bottom channel current is much smaller. When Vgl is +0.5 V, the bottom channel current is comparable to the upper channel current at high Vgu and also dominant at low Vgu. It is noted that the bottom channel current itself in each case is also controlled by Vgu and decreases as Vgu does.

Fig. 4 shows I-V characteristics of an experimentally fabricated device. It can be seen that comparable amount of drain current is controlled by varying one of upper or bottom gate bias voltage.

It is concluded that the XMOS transistor has excellent characteristics for a submicrometer channel length device and for a basic element in 3D-IC's and also in future submicrometer 3D-IC's.

REFERENCE

[1] T. SEKIGAWA and Y.HAYASHI, Solid-State Electron., 27, 8/9, 827(1984).

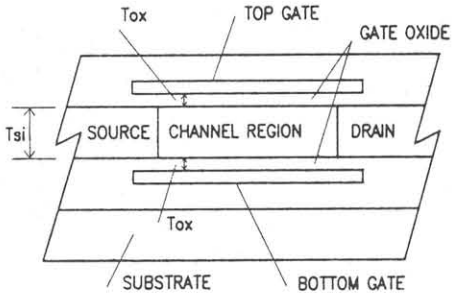

Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

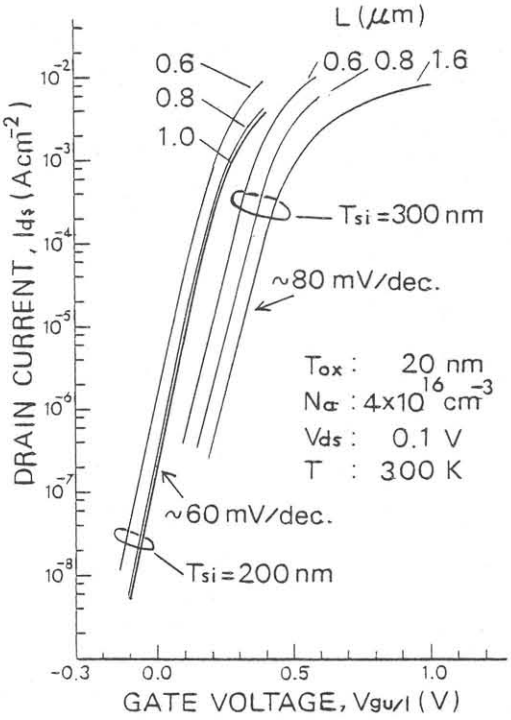

Fig. 2. Calculated subthreshold characteristics of XMOS transistors with the same upper and bottom gate oxide thickness. Vgu = Vgl in this case.

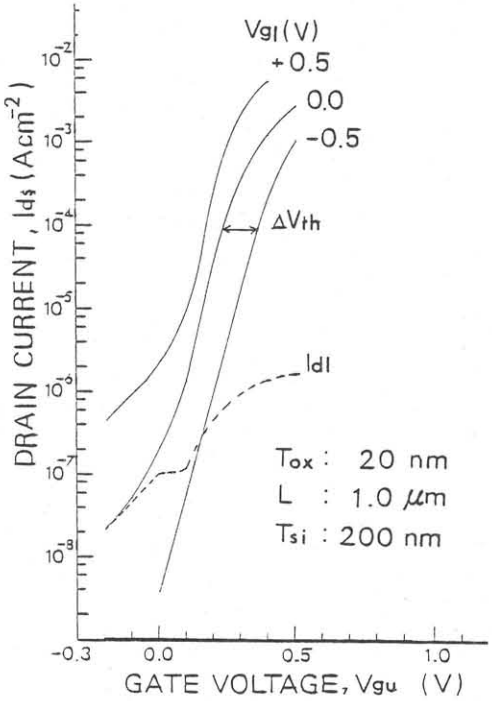

Fig. 3. Calculated subthreshold characteristics of an XMOS transistor. Tsi = 200 nm, L = 1 μm, Toxu = Toxl = 20 nm and Vgl is taken as a parameter.

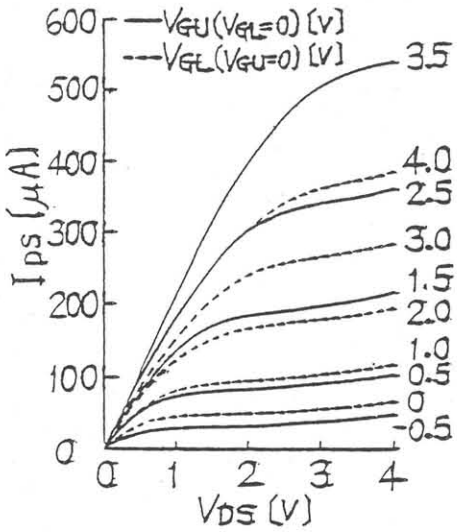

Fig. 4. I-V characterisics of an experimentally fabricated XMOS transistor. Gate length is 2 μm. Upper and lower gate oxide thickness are 20 nm.