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Negative Differential Resistance in CHIRP Superlattice Diodes

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In this news, we report the observation of negative differential resistance (NDR) in CHIRP (Coherent hetero-interfaces for reflection and penetration) superlattice diodes.

The CHIRP superlattice is a stack of alternating thin layers of two different semiconductors with monotonically varying layer thickness[1]. The modulating period in this superlattice is designed to produce graded miniband as shown in Fig. 1. The CHIRP diode consists of this superlattice, an emitter at one end and a collector at the other end. The conduction band edge of the emitter is designed so that the electron impinging against the superlattice falls into its minigap. The electron must tunnel the minigap to traverse the superlattice. The slope of the minigap and, consequently, the barrier thickness for the tunneling vary by the applied electric field. The barrier becomes thickest when the particular electric field is applied to make the first minigap lie horizontally. In this condition the impinging electron has only the small chance for tunneling, resulting in high resistance for the diode. The diode has lower resistance at higher or lower electric field, since the electron has larger chance for tunneling compared to this extreme condition. In this way, this device exhibits NDR characteristics. It should be noted that the CHIRP superlattice obtains high electron reflectivity by the thickness of the barrier of minigap. For the double barrier tunneling device, it was caused by the large barrier height[2]. For the conventional superlattice, it was caused by the wide minigap[3]. Since the CHIRP superlattice has low (typically 100meV for liquid nitrogen operation) barrier height and narrow (about 66meV) minigap, parasitic realization of the NDR by double barrier tunneling or of conventional superlattice is considerably difficult.

The $Al_{0.1}Ga_{0.9}As$/GaAs CHIRP superlattice diodes were fabricated. Precise control of the superlattice growth was necessary. Among many modes of the fluctuation from the designed parameters, the cumulative error of the layer thickness is most deteriorative to the device performance. To get monolayer thickness accuracy for the crystal growth, the newly developed PLE (Phase locked epitaxy) method of MBE growth[4], which makes use of the real-time analysis of RHEED intensity oscillation, was employed. Diodes of 4um in diameter were fabricated on this wafer. Its cross-sectional view is shown in Fig. 2.

The I-V characteristics of the CHIRP diode at 85K is shown in Fig. 3. The NDR is observed when the emitter is negatively biased, whereas no NDR is observed in the reversely biased condition. This asymmetry is characteristic of the CHIRP diode[5], and should not be observed in a double barrier diode nor conventional superlattices. The bias voltage for the NDR is significantly larger than its theoretical value (-0.3V). This may be attributed to the non-uniform electric field across the superlattice caused by the space charge in it.

This is a demonstration of the quantum-mechanical interference effect for electrons in the superlattice structures, where all

barrier layers have lower energy than the impinging electrons and, therefore, no reflection for electrons is expected from the classical mechanics.

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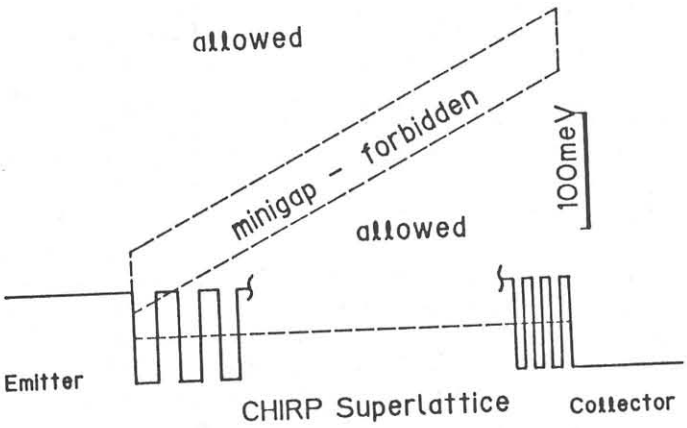

Fig. 1 Band (solid line) and miniband (broken line) structure of the CHIRP diode

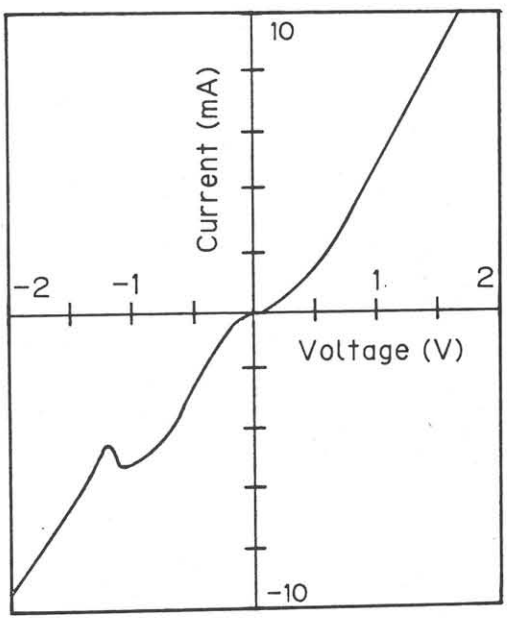

Fig. 3 I-V characteristics of the CHIRP diode

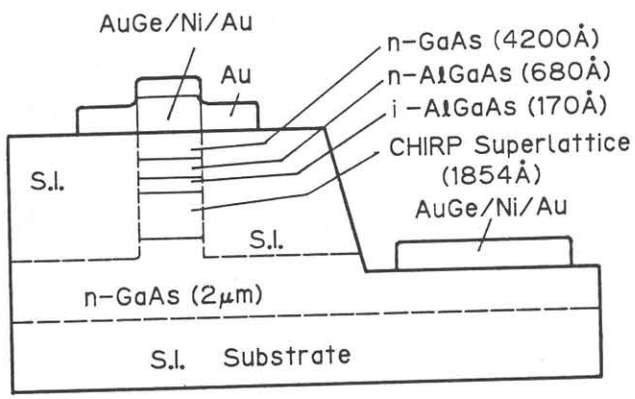

Fig. 2 Cross-sectional view of the CHIRP diode