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High Aspect Ratio Hole Filling with CVD Tungsten for Multi-level Interconnection

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Newly developed processing for high aspect ratio (about 3) hole filling by W-CVD combined with Si sidewall technique and resist etchback is proposed. Moreover, a novel $W/TiN/TiSi_2$ structure is proposed in order to suppress rapid silicidation of W at temperatures higher than 800°C.

1. Introduction

For realizing reliable quarter micron VLSI and three dimensional LSIs , planarizing the interlevel insulator and filling high aspect ratio holes with metal are indispensible. RF bias sputtering[1] , selective CVD W[2-4] and blanket CVD W/WSi_2 [5] combined with in situ etch-back to form planarized via-hole filling have been reported. However, complete hole filling without voids for an aspect ratio over one has not yet been reported.

In this paper, a newly developed processing for high aspect ratio (about 3) hole filling by W-CVD combined with Si sidewall technique and resist etch back is proposed. The underlying layer can be any conductive material and can be applied to filling holes of various depths at the same time. Moreover, a novel $W/TiN/TiSi_2$ structure was applied in order to suppress rapid silicidation of W at temperatures higher than 800°C.

2. Experiments

Selective and non-selective tungsten or W silicide was deposited in a cold wall LPCVD reactor with a heated susceptor. The samples were finally dipped in 1 % - HF solution before being set in an equipment. Four kinds of reaction were performed, as follows.

$$2WF_6 + 3Si \longrightarrow 2W + 3SiF_4 \quad (1)$$
$$2WF_6 + 3H_2 \longrightarrow 2W + 6HF \quad (2)$$
$$WF_6 + 3/2\ SiH_4 \longrightarrow W + 3/2\ SiF_4 + H_2 \quad (3)$$
$$WF_6 + 2SiH_4 \longrightarrow WSi_2 + 6HF + H_2 \quad (4)$$

All depositions were performed at substrate temperatures between 360-500°C. The filling process is shown in Fig. 1. First, 300-1000 Å poly Si sidewall was formed inside the deep hole by using poly Si deposition with LPCVD and etching back by RIE. Second, 500 Å selective W was deposited by reaction (1). Third, 700-800 Å W-Si alloy was deposited by reaction (4) for adhesion improvement. Finally, about 1 μm blanket W was deposited by reaction (2) or (3). Photoresist was employed as planarizing material and etched off together with the underlying metal layer.

For high temperature annealing, $TiN/TiSi_2$ was employed as a reaction barrier layer between W and Si. TiN was deposited by reactive sputtering Ti target in N_2 and Ar. $TiSi_2$ was sputtered by a composite target.

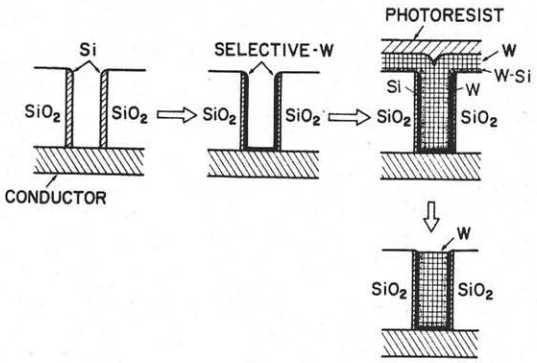

Fig.1 Process sequence of via-hole filling.

3. Results and discussion

Fig. 2 shows the ratio of minimum sidewall thickness to top tungsten thickness as a function of the aspect ratio of the hole measured by SEM observation. Hole depth was 2.2 μm. The step coverage over the hole was better for reaction (2) (150-200 Å/min) than for a reaction (3) (1000-1500 Å/min). Deposition temperature was 380°C. A slower deposition rate is considered to be better for step coverage, since the stagnant layer thickness would become thinner for slower deposition rates. Therefore, the blanket W was deposited by reaction (2). Fig.3 shows a cross-sectional view of a hole filled with CVD-W. Hole depth and width were 2.2 μm and 0.75-0.8 μm, respectively. The aspect ratio of the contact hole was about 3. No void was observed by SEM as shown in Fig. 3. The filling W / Si contact property was examined for 0.75-1.6 μm contact size of with 2.2 μm hole depth. For the N^+ Si, As concentration at the surface was 2.5×10^{20} cm^{-3} and for the P^+ Si, Boron concentration was 2×10^{20} cm^{-3}. Fig. 4 shows that the contact resistivity was below 1×10^{-6} $\Omega \cdot cm^2$ even for a submicron contact hole after annealing at 600°C for 60 min.

Tungsten is known to react with Si to form W silicide above 650°C [6]. In order to suppress silicidation of W , $TiN/TiSi_2$ barrier layer was interposed between W and Si. The reduction in free energy by nitridation is larger for Ti than for W , therefore, W/TiN interface is stable.

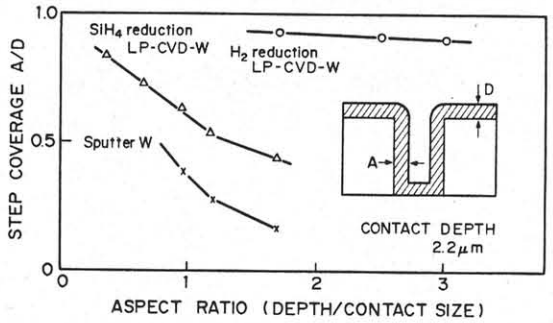

Fig.2 Step coverage for tungsten as a function of the hole aspect ratio.

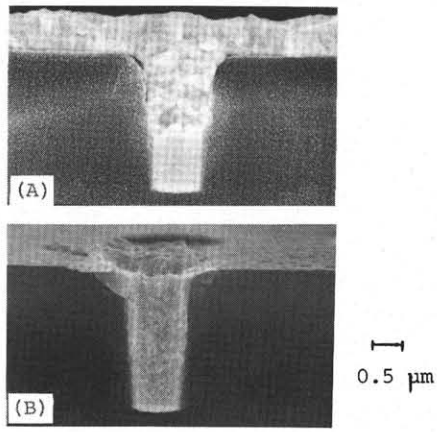

Fig.3 Hole filling with CVD-W. (A) During etching (B) After etching.

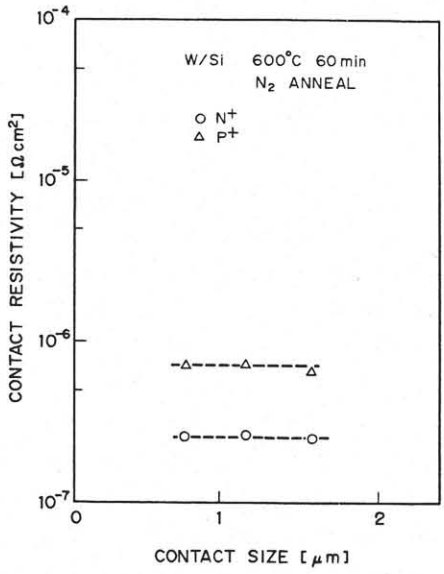

Fig.4 Contact resistivity of W/Si contact after 600°C annealing, as a function of contact size.

Fig. 5 shows the X-ray diffraction pattern of $W/TiN/TiSi_2/Si$ structure after annealing at 600-950°C for 30 min. W did not react with Si even after annealing at 900°C for 30 min.

The W/Si system reaction rate is examined by Taly-step measurement and the X-ray diffraction peak height of body centered cubic (110)W. W has a strong (110) preferred orientation. Since W absorbs Cu Kα X-ray, the W(110) peak (2θ = 40.3°) intensity is measured as a function of tungsten thickness. The results is shown in Fig. 6. The theoretical curve was calculated from the linear absorption coefficient (170.5cm^2/g) and density (19.3 g/cm^3) of W. The theory and experimental results match shows the validity of the silicidation rate evaluation. Fig. 7 shows the reaction rate for the W/Si and W/TiN/TiSi$_2$/Si systems. The silicidation rate is plotted as the W reaction rate. Activation energy values were 2.9 eV and 2.29 eV, respectively.

This difference means that the reaction limiting process for the latter system is not a W/Si reaction. The limiting process is considered as Si supply through the TiN/TiSi$_2$ layer. The Si supply was accomplished by diffusion through localized defective spots in TiN layer. The reaction rate with barrier layer is 2-2.5 orders of magnitude lower than W/Si system. Fig. 8 shows SIMS in-depth profiles for W, Ti, Si and B after annealing at 900°C for 30 min. No Si atoms were found in the W layer, which means that tungsten silicidation did not occur. Boron outdiffusion was also suppressed by TiN layer. 0.9 - 1.0 x 10^{20} cm^{-3} boron concentration at the Si surface was not changed after annealing.

In Fig. 9 the contact resistivity dependence on annealing temperature is shown. Without the reaction barrier, the contact resistivity between W and Si abruptly increased above 800°C, due to rapid consumption of the highly doped Si layer. By using the TiN/TiSi$_2$ layer, the Si transport was found to be suppressed and the contact resistivity below 1x10^{-5} Ω·cm^2 was obtained at 900°C for 30 min.

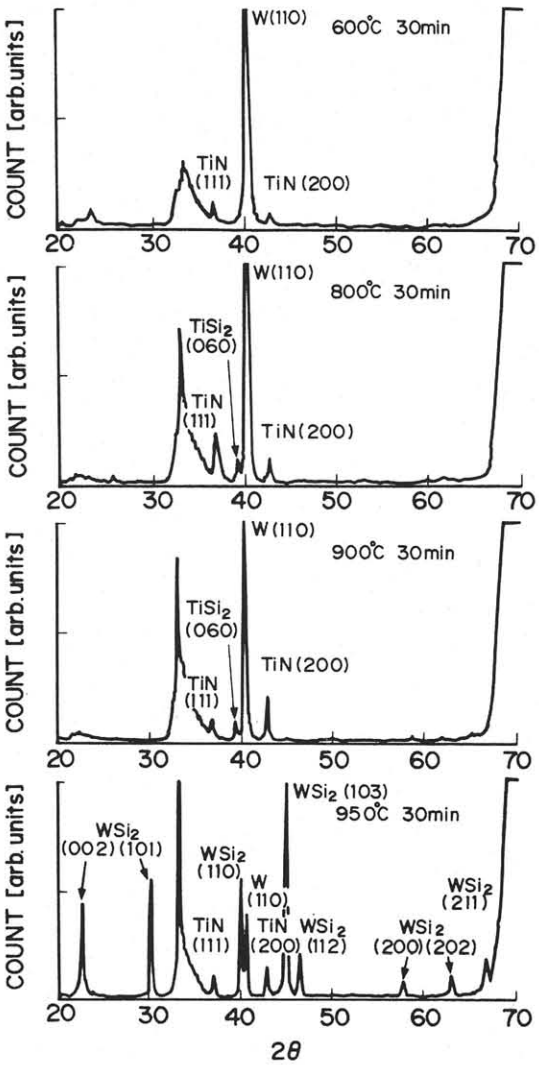

Fig.5 X-ray diffraction pattern for W/TiN/TiSi$_2$/Si after isochronal annealing at 600-950°C for 30 minutes.

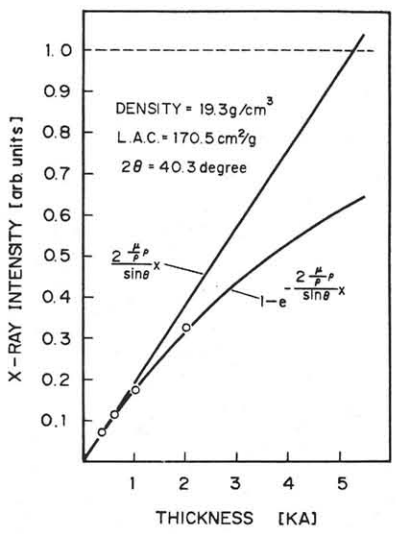

Fig.6 X-ray intensity of (110)W peak as a function of W thickness.

4. Summary

A process for high aspect ratio via-hole filling is proposed. By using W-CVD combined with Si sidewall and resist etch-back, a hole with aspect ratio of 3 was completely filled. The contact property of the filling W/ Si shows very low contact resistivity after annealing at 600°C-700°C. After high temperature annealing at higher than 800°C , the TiN/$TiSi_2$ barrier layer was found to be effective. Good ohmic contact was obtained, even after annealing at 900°C for 30 min without W silicidation.

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5. References

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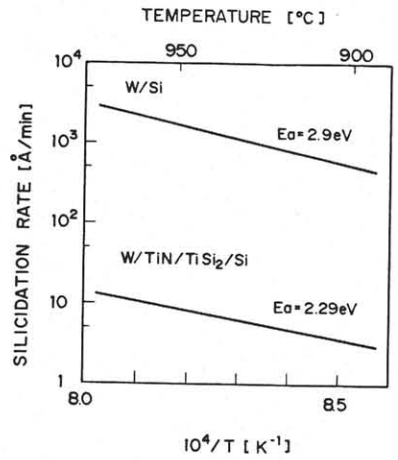

Fig.7 Tungsten reaction rate as a function of 1/T.

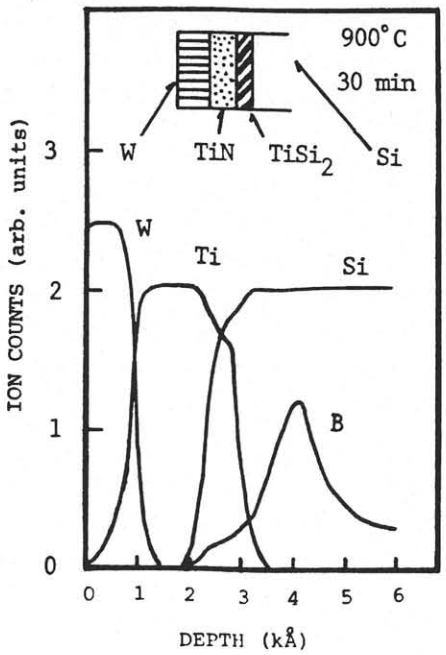

Fig.8 SIMS in-depth profiles for W, Ti, Si and B for W/TiN/$TiSi_2$/Si system after annealing at 900°C for 30 minutes.

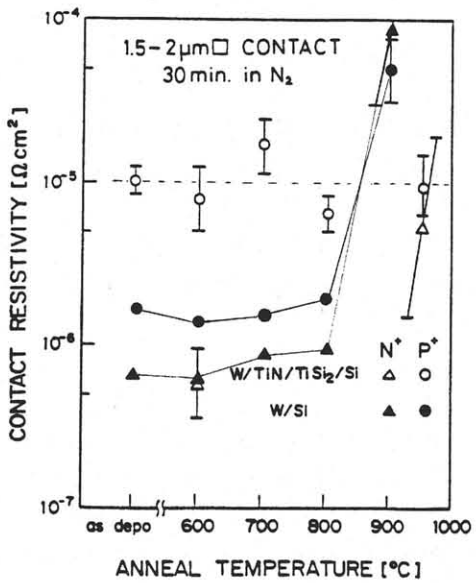

Fig.9 Contact resistivity as a function of annealing temperature.