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Plasmask: A Novel Plasma Developed Resist Based on Selective Silylation

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A new resist system called PLASMASK, using the DESIRE process is described. The DESIRE process is based on the selective silylation of a thin top layer of the exposed resist areas. The silicon which is thus incorporated into the exposed areas renders these areas resistant to a reactive oxygen plasma by the in situ formation of a SiO2 mask. In this way multilayer performance can be obtained with a single layer resist process. By using a two-step development process, contrast enhancement can also be obtained.

1. Introduction

As a result of the increase in density of very large scale integrated circuits, the minimum feature size of semiconductor devices is decreasing, and the production processes are becoming more and more difficult. Achieving micron and submicron resolution, with sufficient linewidth control on substrates with reflective topography, is becoming a major problem. Resolution problems on topography can be basicly divided between the bulk effect and reflection problems.

The bulk effect is a consequence of the light absorbance of the resist material. This results in a decrease in exposure energy at the bottom of the resist compared to the top. This, combined with the isotropic character of wet development, gives rise to sloped resist profiles. When the sidewalls of a resist pattern are not vertical, the linewidth will depend on the resist thickness, and thus linewidth variations are inevitable when a small line crosses a step in the substrate.
When the light can be reflected at the substrate, the reflected light will interfere with the incident light, resulting in standing waves. The effect thereof can be seen as a scalopping of the resist sidewalls.
When the position of the nodes is such that a minimum in exposure energy is located near the resist-substrate interface, incomplete development and scumming may occur.
In addition, reflection of light at the edges of topography may cause reflective notching effects.

High resolution is not the only requirement for submicron resists. Since dry etch techniques are used for the pattern transfer, high thermal stability, and resistance to a harsh plasma environment are crucial.

One way of solving all these problems is the use of multilayer resist schemes which were introduced by Havas[1-3] in 1973. Very good results were obtained with the trilayer process. The advantage is that the thermal stability, etch resistance and planarization of a thick bottom layer can be combined with the high resolution of a thin resist layer on a quasi flat surface. With an intermediate layer of e.g. spin-on-glass, vertical transfer of the patterns in the thin imaging layer into the thick bottom layer can be carried out, using an anisotropic oxygen plasma (RIE). Since the profiles obtained are vertical, and the bottom layer can be dyed in order to absorb reflected light (4), no bulk effect or reflective notching is to be expected, and excellent linewidth control is possible, even over highly reflecting steps.

However, there are several drawbacks to multilayer systems. The process is too complicated to be used in production lines. In addition, stress and the formation of interfacial layers occurs when layers of different materials are coated on top of each other and baked.
Finally, applying a uniform and pinhole-free thin coating of resist as top layer is not always an easy task.

2. The DESIRE process

The ideal system would obviously be a single layer resist affording the outstanding performance of multilayer resists systems, but without any of their drawbacks.
It is thus not surprising that many attempts have been made to achieve this goal. A first step in this direction is the bilayer/RIE

scheme using a silicon containing resist as imaging layer. Many systems have been described recently, but none of them has been realy succesfull thus far.(5-8)
Wolf et al from AT&T(9) and MacDonald et al(10) from IBM described so called pseudo-monolayer systems, in which, after exposure, an inorganic gas is incorporated in either the exposed or the unexposed areas.
However, poor selectivity of the AT&T system results in excessive residu formation and loss of residual resist thickness. With the IBM system, submicron resolution was obtained using deep UV or X-ray exposure, but the system is not sensitive to near UV exposure, which makes it useless for existing exposure tools with sufficient alignment accuracy.
The PLASMASK resist system, however, is a real pseudo-monolayer system designed to be used on near and mid-UV steppers (g,h and i-line). The complete process, called DESIRE,(11-12), is shown in figure 1.

Only one single layer of resist is spin-coated on the substrate, (1a), and prebaked to a self-planarizing layer. After patternwise exposure, (1b), on standard exposure equipment, the wafers are treated with a vapourized silylating agent. (e.g. HMDS).

As a result of the photochemical modifications of the resist during exposure, the exposed areas are selectively silylated,(1c), in such a way that silicon is incorporated into the top 100 - 150 nm of these exposed parts. In the last step the wafers are developed in an oxygen plasma whereby the silicon is converted into silicon dioxide, (1d). This forms a thin protective mask that stops etching in these areas. The unexposed parts do not contain silicon and are removed during the development (1e). When an anisotropic plasma is used for the development, vertical resist profiles are obtained.

Since silicon is incorporated only in a shallow top layer of the resist, light does not need to penetrate to the substrate during exposure. In this way, reflection from the substrate can be suppressed. This will avoid standing wave effects and reflective notching on topography. Moreover, since the exposure takes place in a thin top layer of a planarized resist coating, depth of focus requirements can be relaxed.

That silicon incorporation is indeed limited to a thin top layer of the resist, has been demonstrated using Auger, SIMS end RBS experiments. From AUGER, silicon depth profiles in the resist as a function of exposure dose could be seen, showing that the penetration depth of the silylating agent depends on the exposure energy. In case of the optimum exposure dose the penetration depth was found to be between 100 and 150 nm.

Since imaging takes place in only a thin, top layer of the resist, resolution is only limited by the exposure contrast of the exposure equipment. On a 0.30 NA GCA stepper (g-line), resolution of 0.7 μm - 0.8μm can be obtained, regardless of the resist thickness and topography. On a g-line stepper with an 0.38 NA lens, 0.6μm lines and spaces have been patterned. When an i-line stepper is used with a high NA lens, resolution down to 0.4 - 0.5μm can be obtained.

In figure 2 a,b and c 2.5, 0.7 and 0.6 μm lines and spaces in Plasmask resist are shown. Resist thickness is 1.3μ m in figure 2a and b, and 2.3μm in figure 5c.

Figure 3a shows 0.7μm lines and spaces on aluminium substrate and figure 3b, 0.6 μm lines in 2.3 μm thick resist over 1μm oxide steps. Figure 4 shows 0.6 and 0.4 μm lines and spaces on 1μm high aluminium topography in 1.6μm thick Plasmask resist, exposed on an i-line stepper.

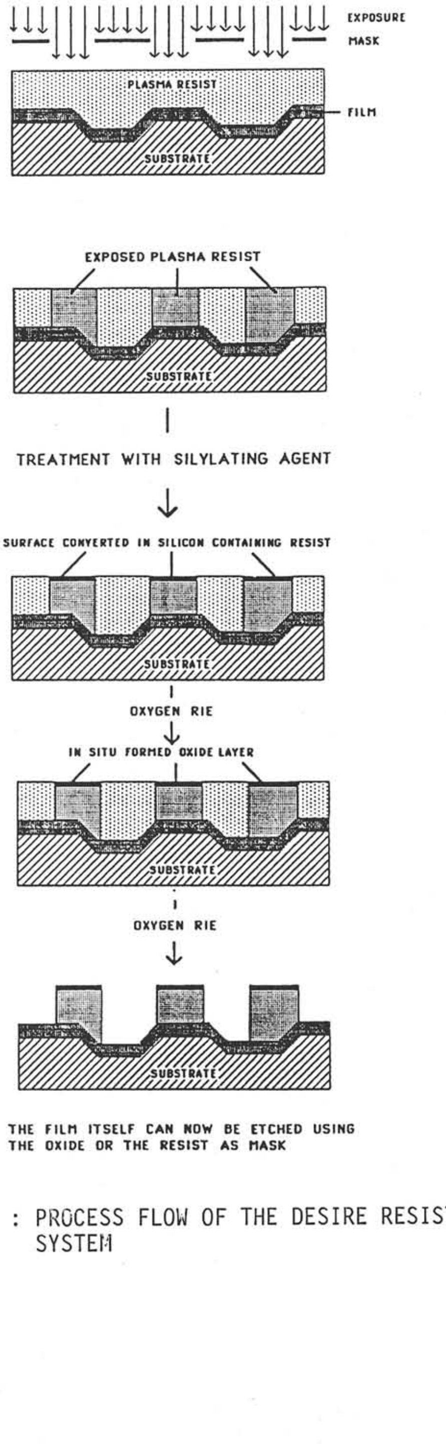


FIGURE 1 : PROCESS FLOW OF THE DESIRE RESIST SYSTEM

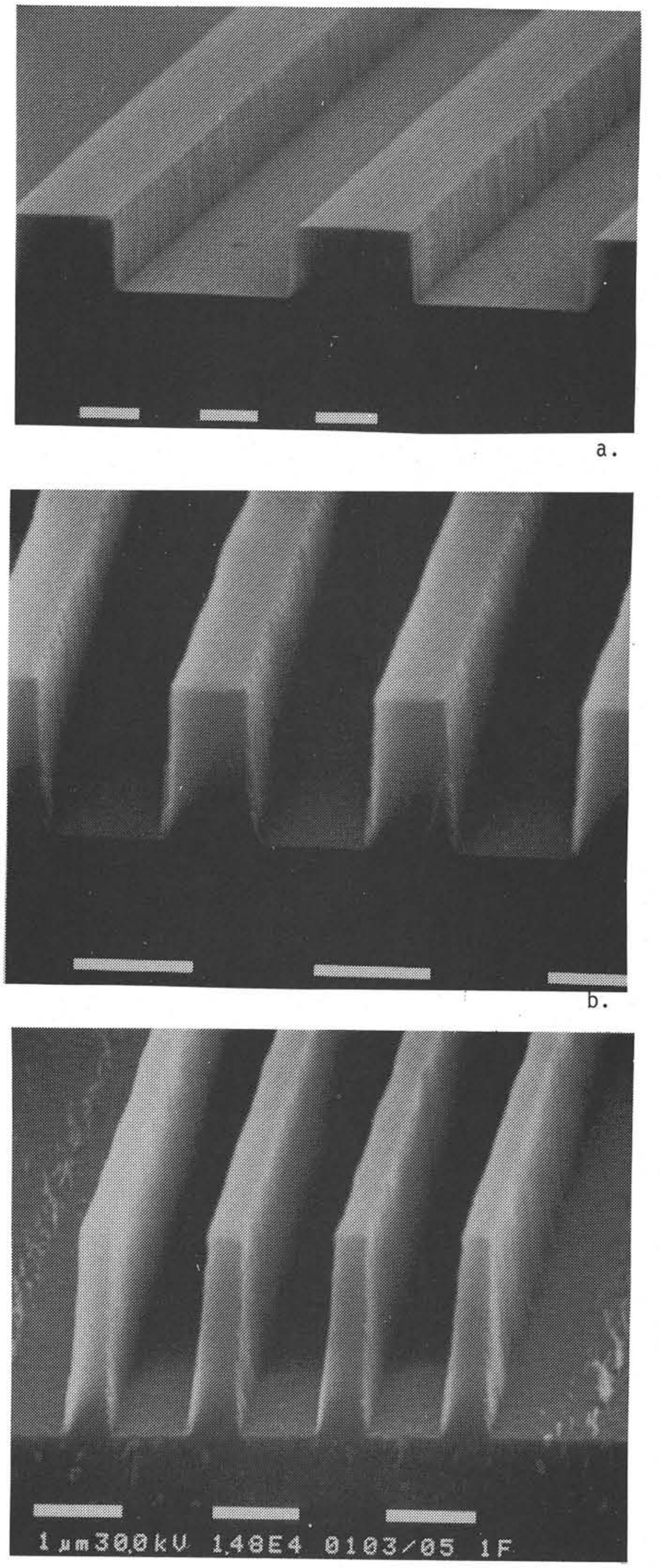
From the AUGER results, it can be concluded that the incorporation of silicon is controlled by diffusion rather than by reactivity. This means that not only the concentration of silicon will be very low in the unexposed areas, but also that the depth of penetration is limited to the surface.
Indeed, as was mentioned above, depth of penetration depends on exposure dose. While in regularly exposed areas silicon is incorporated to a depth of up to 150 nm, the slight exposure resulting from diffraction in the unexposed areas causes silylation only in the top 5 to 10 nm. This gives us the opportunity to remove this thin layer with a non-selective process. The easiest way of doing this is using a two-step development process. In a first, short step, a plasma with oxygen combined with a fluorinated gas (e.g. C_2F_6, CF_4, SF_6,...) removes the thin layer containing some silicon in the unexposed areas but it also results in contrast enhancement. When the thin upper layer is removed, the frontier between silylated and non-silylated resist is defined by a much steeper silicon profile.

That contrast enhancement does occur in a two step process is demonstrated in figure 5. Here it can be seen that by simply raising the C_2F_6-flow in the first development step from 0 to 5 sccm the contrast is increased from 2.4 to 5.6 !

Finally the thermal stability of the Plasmask material was evaluated. From figure 6 it can be seen that hot-plate baking at temperatures up to 300°C does not cause any deformation of the resist patterns.

3. CONCLUSION

A new resist material and process has been described enabling submicron resolution on reflecting topography with excellent linewidth control. Since imaging takes place in a thin, top layer of the resist and the coating can be made highly absorptive, multilayer-like performance is obtained, without any of its disadvantages. The number of processing steps is equal to a standard wet developed resist, no stress or intermixing problems occur, and instead of spin coating a thin top resist layer, a thin upper layer of the thick Plasmask layer is used, resulting in pinhole-free coating. Because of the complete reduction of reflected light, linewidths are independent of resist thickness. This relaxes the requirements of coating uniformity dramatically, which may become a major advantage for large wafer sizes. Also, focussing is less critical since the imaging layer is very thin and planar. Finally, by using a two-step development process, contrast enhancement may be obtained. We may thus conclude that in the DESIRE process we combine a tri-layer and contrast enhancement in a single layer resist process.



c.

Figure 2 : Dry developed patterns in Plasmask resist.
a: 2.5 μm lines and spaces in 1.3 μm thick resist.
b: 0.7 μm lines and spaces in 1.3 μm thick resist.
c: 0.6 μm lines and spaces in 2.3 μm thick resist.

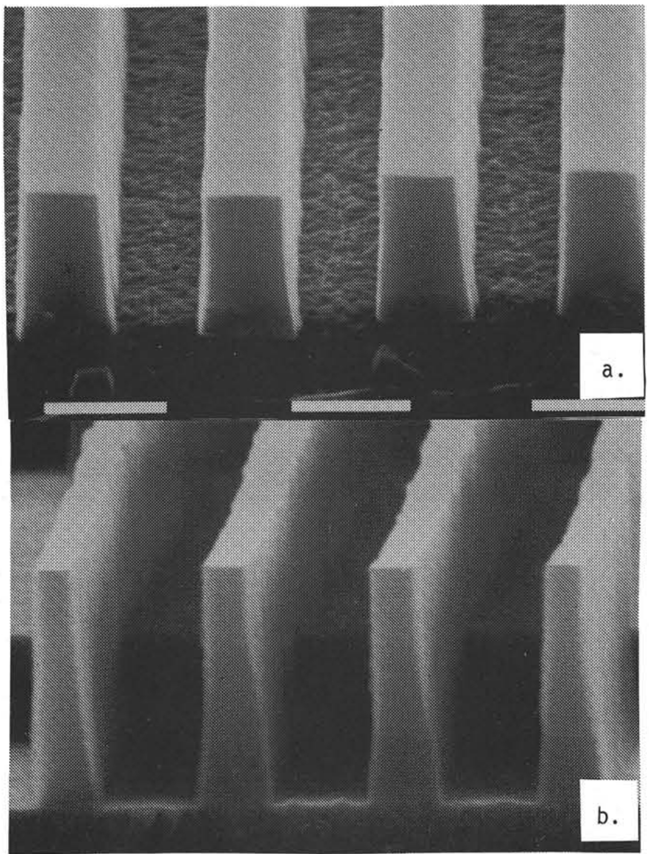


FIGURE 3 : Dry developed patterns in Plasmask resist.
a: 0.7 μm lines and spaces on aluminium substrate
b: 0.6 μm lines and spaces on 1 μm oxide steps.

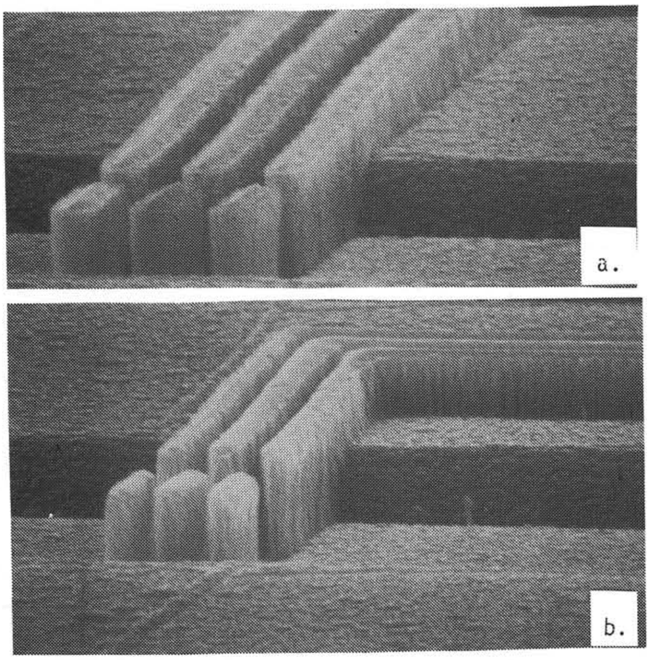


FIGURE 4 : Plasmask resist patterns (i-line exp) on 1 μm aluminium topography
a : 0.6 μm l/s
b : 0.4 μm l/s

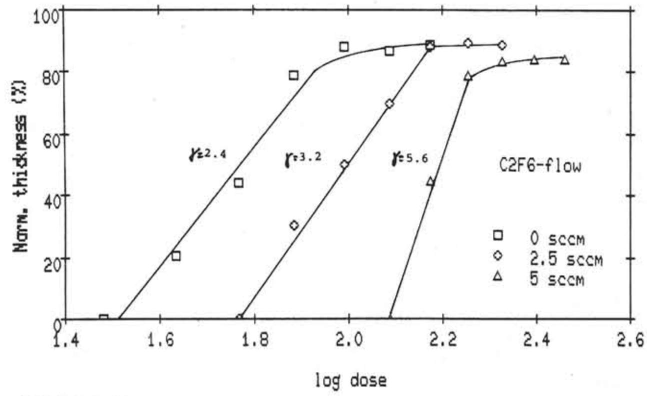


FIGURE 5 : contrast curves for different C_2F_6 - Flows

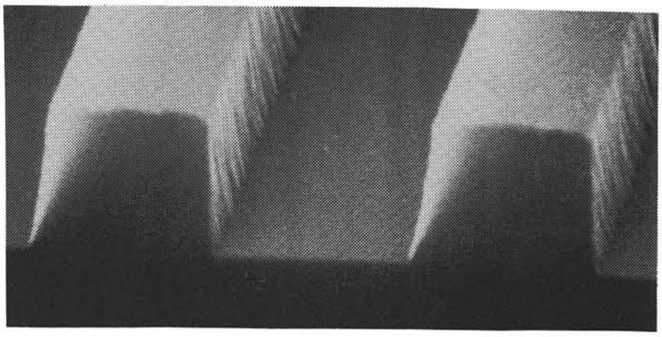


FIGURE 6 : Plasmask pattern after 300°C Bake

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