Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 53-56

Low Temperature Low Pressure Silicon Epitaxial Growth and Its Application to Advanced Dielectric Isolation Technology

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Increased usage of epitaxial structures in various advanced bipolar and MOS submicron device technologies have led to significant breakthroughs in conventional CVD epitaxial processing techniques. These breakthroughs are due to the realization of low temperature (826°C) low pressure (<25 torr) SiH_2Cl_2 epitaxial growth. High resistivity P/P^+ and N/N^+ CMOS epilayers of excellent crystal quality with epi/substrate transition region widths as narrow as 400 Å have been achieved. Also, high quality lateral dielectric isolation by Selective Epitaxial Growth (SEG) and vertical isolation by Selective Poly Deposition (SPD) and Epitaxial Lateral Overgrowth (ELO) have been realized.

1. Introduction

With the continued scaling of device structures to the submicron level, two key areas of concern in using epitaxial structures are; 1) how to minimize the epi/substrate transition region width (due to autodoping and solid phase diffusion) and 2) the appropriate dielectric isolation technology for lateral and vertical isolation when using an epitaxial structure. Recently, much attention has been focused on low temperature single crystal silicon epitaxial growth which has very abrupt epi/substrate transition region width to achieve very thin epitaxial structures. For advanced bipolar device fabrication, transition widths of <0.3 μm with total epilayer thickness of 0.8 μm is desirable. In CMOS technology, submicron transition width and total epilayer thickness of <2 μm will be necessary. Autodoping from the buried layer structure (bipolar devices) or heavily doped substrate (CMOS devices) and dopant diffusion during epitaxial growth at high temperatures influence the epi/substrate transition region width and thereby limit the epilayer thickness. Historically, low temperature silicon epitaxial growth (temperatures below 1000°C) has been achieved by CVD techniques in the SiH_4/H_2 system or by Molecular Beam Epitaxy (MBE) and Plasma Enhanced CVD (PE-CVD) growth techniques (1, 2). Both of these techniques produce single crystal silicon epitaxy with very abrupt epi/substrate transitions; however, the epilayer quality is only moderate. High density of dislocations ($>10^3/cm^2$), impurities and deep level traps have been observed in the epilayer. In this report we will present our recent results on high quality silicon epilayer growth at temperatures as low as 826°C in the SiH_2Cl_2/H_2 system in a commercially available AMC-7800 RPX epi-reactor at pressures as low as 8 torr.

2. Low Temperature Epitaxy

Low temperature (826°C) deposition of single crystalline silicon epitaxial layers has been achieved from the decomposition of SiH_2Cl_2 at pressures as low as 8 torr in the epi-reactor. A plot of growth rate versus temperature for SiH_2Cl_2 deposition at 25 torr is shown in Figure 1. At a temperature of approximately 925°C the epitaxial growth kinetics changed from gas phase diffusion to surface reaction rate limited growth. Above 925°C the growth rate is limited by gas phase diffusion, therefore it is independent of temperature. Below 925°C the growth rate is limited by surface reaction kinetics, therefore it is strongly dependent on temperature. At 826°C a growth rate of 0.04 μm/min was measured.

The crystalline quality of these epilayers was examined by various techniques. Electron channeling pattern analysis was used to determine the crystallinity of the epilayers (See Figure 2). The combination of low temperature with low pressure was required to achieve low temperature single crystal epitaxial growth. Wright etching to delineate crystallographic defects present in the epilayers showed that the best results were obtained on intrinsic gettered epi-wafers (3). The defect count on 100mm P/P^+ gettered epi-wafers was three to four defects per wafer and for N/N^+ gettered epi-wafers, four to six defects/cm^2. MOS capacitor C-t lifetimes on Pre-Epi intrinsic gettered N/N^+ epi-wafers varied from 55 to 791 μsec with the average being 363 μsec. This was higher than that typically observed on standard N/N^+ epi-wafers obtained from several different silicon suppliers. Also, standard P/P^+ and N/N^+ epi-wafers purchased from silicon suppliers typically yield 40% to 80% on oxide leakage measurements and the 826°C, 20 torr non-gettered P/P^+ epi-wafers yielded 69%, while the Post-Epi intrinsic gettered P/P^+ epi-wafers yielded 81% and the Pre-Epi intrinsic gettered N/N^+ epi-wafers yielded 87%.

Boron autodoping and epi/substrate transition region widths were determined by Secondary Ion Mass Spectrometer (SIMS) and Spreading Resistance Profile (SRP) analysis. For P/P^+ CMOS epitaxial structures, boron autodoping was reduced by over 1.5 orders of magnitude from 5.5×10^{15} down to 1.5×10^{14} boron atoms/cm^3 and the transition region width was as narrow as 416 Å (See Figure 3).

This growth technique eliminated the need to backside seal P^+ substrates used in CMOS technology. For N/N^+ CMOS epitaxial structures, the transition region width was as narrow as 400 Å for a 2.5 μm thick epilayer (See Figure 4). For comparison, an N/N^+ epitaxial structure grown by MBE at 750°C is shown in Figure 5. The sample was 1/5 the thickness of the epi-wafer in Figure 4 (~0.55 μm), and the transition width was 125 Å. Also, very good buried layer pattern transmittance were observed at 826°C, 8 torr growth condition.

3. Dielectric Isolation

Several other attractive applications of low temperature low pressure silicon epitaxial growth techniques are in the area of new advanced dielectric isolation techniques. Historically, local oxidation of silicon (LOCOS) has been the process used to dielectrically isolate devices. However, the scalability of LOCOS is limited to about 2 microns in device separation due to lateral oxidation under the nitride mask (bird's beak encroachment) Also, the LOCOS process is usually a high temperature wet oxidation anneal which can result in oxidation induced surface stacking faults (OISF) and dopant redistribution which leads to a broadening of the epi/substrate transition region width. Through the application of low temperature, low pressure SiH_2Cl_2 epitaxial growth techniques a new lateral isolation technique and two new vertical isolation techniques have been realized.

The application of Selective Epitaxial Growth (SEG) for lateral dielectric isolation in MOS, bipolar, Bi-MOS and CCD technologies has been successfully achieved, making it a very attractive alternative to LOCOS (4-11). Devices with SEG isolation structures have been fabricated using a high density MOS production line process (11). A comparison of surface topography after 2nd level poly between a LOCOS isolated device and an SEG isolated device is shown in Figure 6. Excellent NMOS transistor characteristics were observed and are shown in Figures 7, 8 and 9. Also, the added flexibility in device processing by using SEG is shown in Figure 10 for a twin tub CMOS technology.

For vertical dielectric isolation, silicon on insulator (SOI) structures have been achieved by two different silicon epitaxial deposition techniques. Selective Poly Deposition (SPD) is shown in Figure 11 where you have elevated source and drain structures (12). Another form of elevated source and drain structure is achieved by Epitaxial Lateral Overgrowth (ELO) shown in Figure 12. Fully vertically and laterally isolated structures can also be achieved by ELO as shown in Figure 13 (6, 13, 14). A cross-sectional TEM micrograph of a 2.5 to 1 lateral to vertical growth ratio ELO structure which is also dislocation free is shown in Figure 14. Figure 15 shows a 10 to 1 lateral to vertical ELO structure grown over a planarized recess LOCOS structure, making this technique a strong candidate for future 3-D stacked CMOS structures.

4. Summary

In summary, ideal epitaxial structures for future submicron device technologies have been achieved by the application of low temperature low pressure silicon epitaxial growth techniques. High quality single crystal silicon epitaxial structures have been grown at temperatures as low as 826°C at pressures as low as 8 torr in commercially available epi-reactors. The transition region width for both P/P^+ and N/N^+ epitaxial structures was as narrow as 400 Å, eliminating any concern of autodoping and solid phase diffusion. Excellent lateral dielectric isolation by SEG has been achieved for a high density MOS technology and vertical dielectric isolation by SPD and ELO are very promising.

5. References

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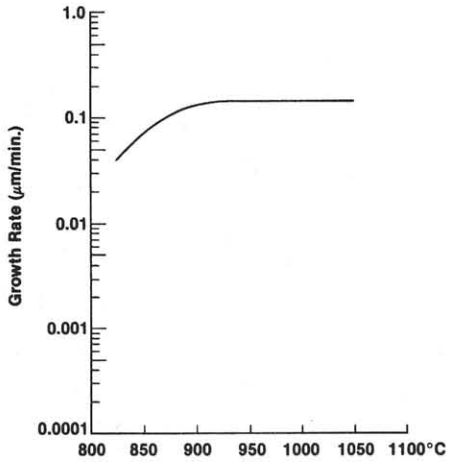
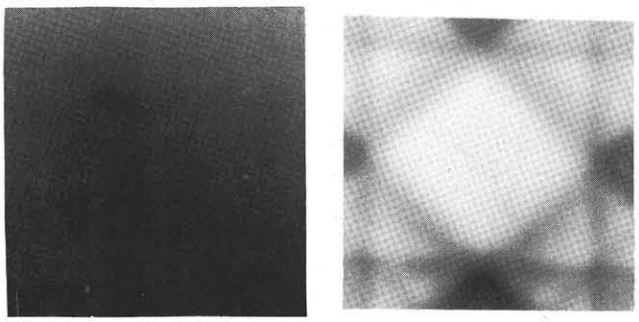


Figure 1: Growth rate-vs-temperature for SiH_2Cl_2 at 25 torr



(a) (b)

Figure 2: Electron channeling pattern of SiH_2Cl_2 epilayer grown at a) 833°C atmospheric and b) 826°C 25 torr

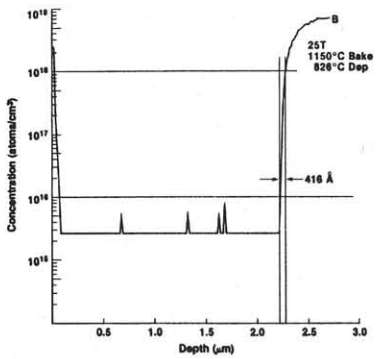


Figure 3: SIMS of P/P^+ 826°C 25 torr

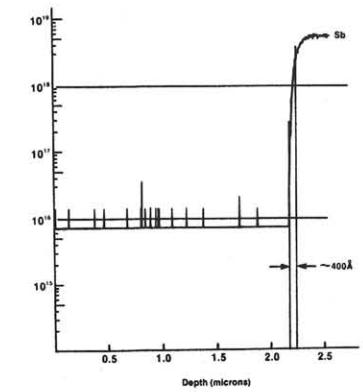


Figure 4: SIMS of N/N^+ 826°C 25 torr

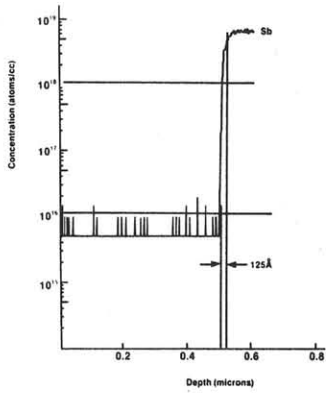
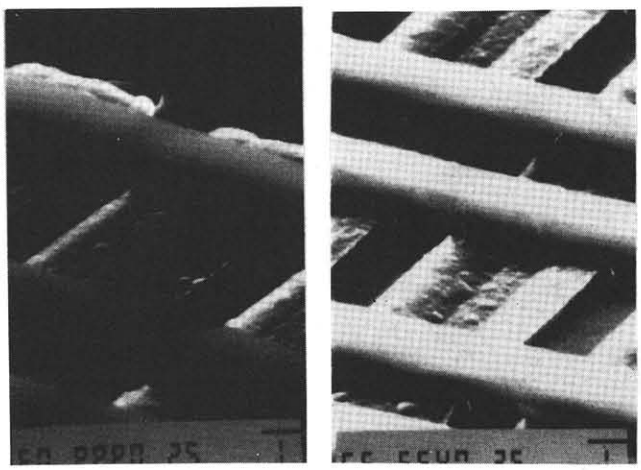


Figure 5: SIMS of N/N^+ 750°C MBE



(a) (b)

Figure 6: Surface topography for a) LOCOS and b) SEG isolated devices

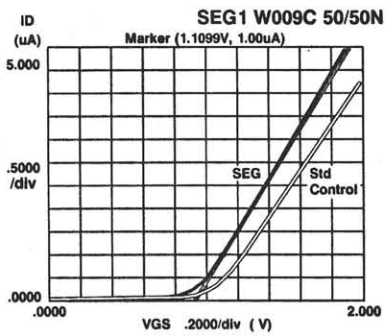


Figure 7: NMOS transistor mobility characteristics

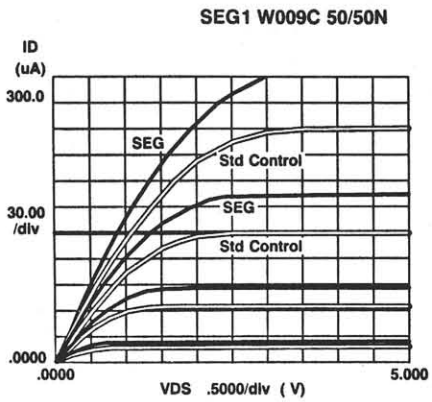


Figure 8: NMOS transistor I-V characteristics

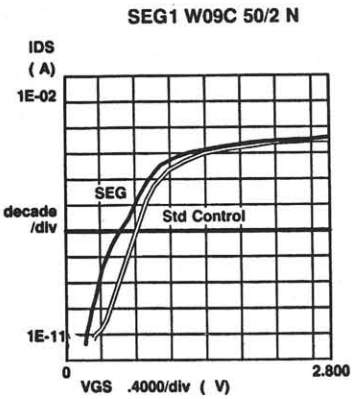


Figure 9:
NMOS transistor subthreshold characteristics

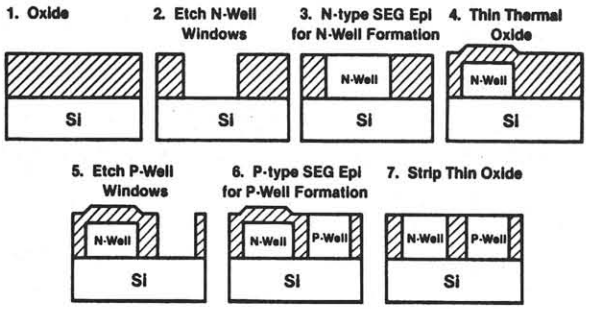


Figure 10: Self aligned Twin Tub CMOS SEG

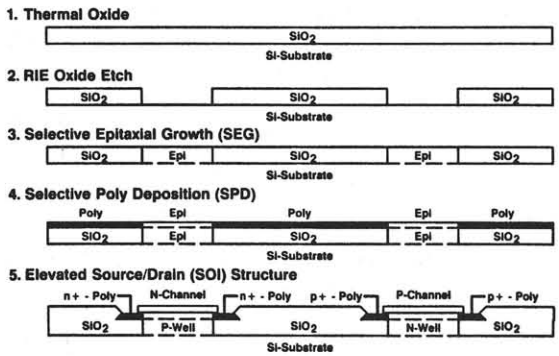


Figure 11: Elevated Source/Drain (SOI) structure by Selective Poly Deposition (SPD)

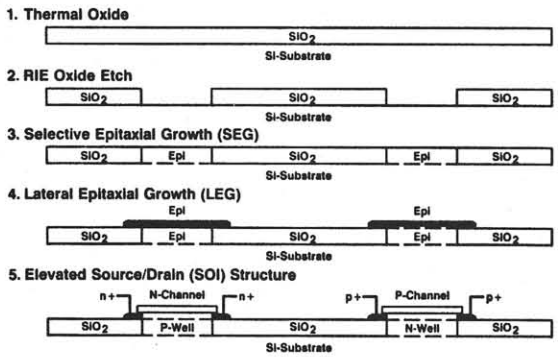


Figure 12: Elevated Source/Drain (SOI) structure by Epitaxial Lateral Overgrowth (ELO)

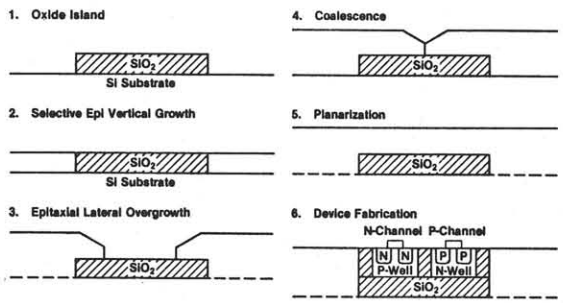


Figure 13: Silicon on Insulator (SOI) by Epitaxial Lateral Overgrowth (ELO)

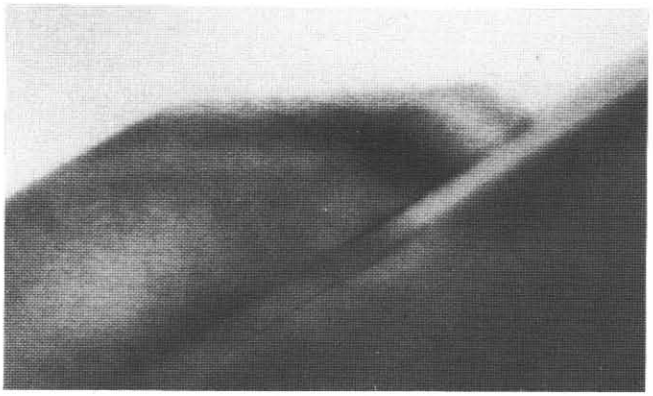


Figure 14: Cross-sectional TEM of 750 Å thick ELO structure

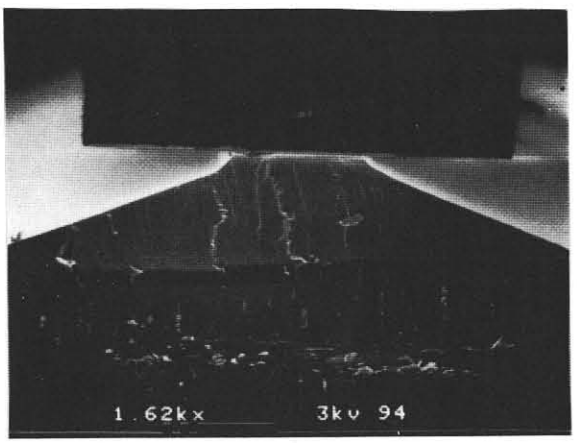


Figure 15: 10 to 1 lateral to vertical ELO growth structure