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The Effect of Post-Oxidation Annealing on Hot- Carrier Trapping Characteristics in SiO_2

Masakazu Shimaya and Noboru Shiono
NTT Electrical Communications Laboratories

3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan

The post-oxidation annealing (POA) effects on hole trapping and electron trapping characteristics in SiO_2 have been investigated using an avalanche injection technique. It is found that a low temperature (around 850°C) POA decreases hole traps but increases electron traps. However, the reverse effect appears under high temperature conditions (above 1000°C) POA. An OH and H diffusing model during high temperature POA is proposed to account for the effect of POA on carrier trapping in SiO_2.

§1. Introduction

It is well known that the injection of electrons or holes into the gate oxide of a MOS device causes the build-up of oxide charges and interface trapped charges, especially when a MOSFET operates in a high electric field[1] or in a radioactive environment[2]. Trapped charges in the gate oxide deteriorate the device performance due to threshold voltage shift. This hot carrier induced instability imposes a serious threat on the reliability of MOS VLSI's.

It is widely recognized that the radiation hardness of a MOS device is significantly affected by the post-oxidation annealing (POA) temperature[3]. However, the physical mechanism of this effect is not well known yet. Also, the POA effect on hot-electron induced instability is not well understood.

In this paper, hole and electron trapping characteristics in SiO_2 have been investigated using an avalanche carrier injection technique, with emphasis on the POA effect on carrier trapping properties.

§2. Experimental

Test devices were poly-Si gate MOS capacitors fabricated on n- and p-type substrates. Highly doped substrates were used to ensure uniform carrier injection into the gate oxide. A 30 nm thick gate oxide was grown in a dry O_2 ambient at 1000°C. The annealing treatment after phosphorous doped poly-Si deposition was carried out at 850, 1000, and 1100°C in a dry N_2 ambient for 60 minutes.

The characterization of carrier trapping in the gate oxide was performed by flat-band voltage (V_{FB}) shift analyses under avalanche carrier injection[4] with a constant current mode at 298 K and at 83 K. Interface trap density (D_{it}) at the Si-SiO_2 interface was measured by utilizing a quasistatic C-V method[5].

MOS capacitors were irradiated with Co^{60} gamma-rays (1.17,1.33 MeV) under various bias conditions in order to investigate the radiation hardness.

§3. Results

3.1 Hole Trap

The V_{FB} shifts as a function of the number of injected holes (N_{inj}) are shown in Fig. 1. The V_{FB} shift for the 850°C annealed sample is extremely small compared with that for the 1000°C and 1100°C annealed samples regardless of injection temperatures. The difference in the V_{FB} vs N_{inj} curves measured at 298 K and at 83 K is very small. The V_{FB} shifts due to gamma-ray irradiation are shown in Fig. 2. Good correlation is also obtained between the V_{FB}

shift due to hole injection and that due to gamma-ray irradiation in regard to POA temperature.

Analysis of the hole injection curves in Fig.1 shows that three kinds of hole traps are present in the oxide. The capture cross-section, σ of the hole trap and the effective trap density, N_{eff} are shown in Table 1. Hole trap densities are very low for the 850°C annealed sample compared with the 1000 and 1100°C annealed sample. Hole trap A with a large capture cross section is detected in only 1100°C annealed sample. Hole trap C with a small capture cross-section is present for the 850 and

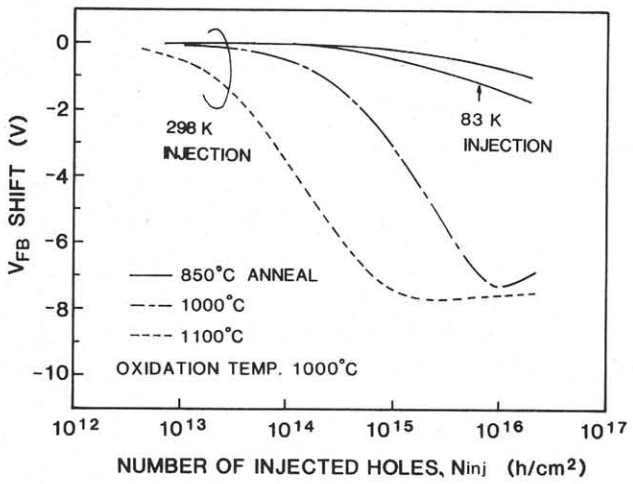

Fig.1 POA temperature dependence of flat-band voltage shifts due to hole injection

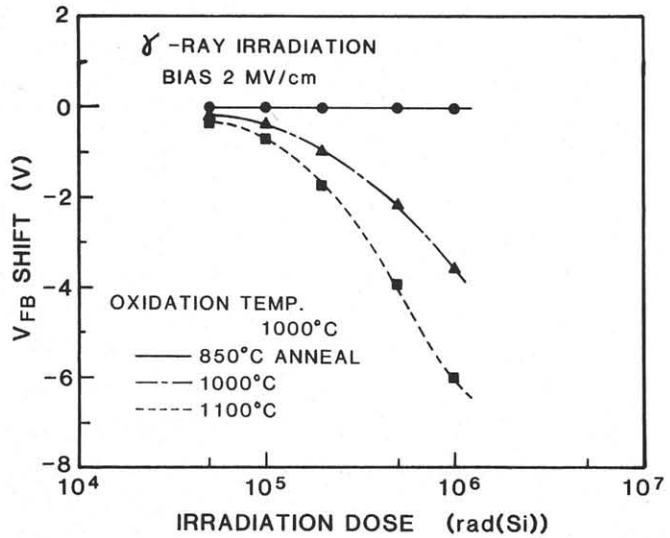

Fig.2 Flat-band voltage shifts due to gamma-ray irradiation under constant gate-bias of 2 MV/cm

Table 1 Values of capture cross-section, σ and effective density, N_{eff} for hole traps evaluated from curves shown in Fig.1

	Capture Cross section	Effective Density, Neff (cm^{-2})			
		298 K Injection			83 K Injection
Trap	σ (cm^2)	850°C	1000°C	1100°C	850°C
A	$1\sim2\times10^{-14}$	--	--	4.1×10^{12}	--
B	$1\sim2\times10^{-15}$	1.8×10^{11}	3.3×10^{12}	2.4×10^{12}	4.1×10^{11}
C	$1\sim4\times10^{-16}$	6.9×10^{11}	3.6×10^{12}	--	1.1×10^{12}

-- Undetected

1000°C annealed samples, and isn't present in the 1100°C annealed sample. This result indicates that a high temperature POA increases the capture cross section of the hole trap. POA affects not only the hole trap density but also the capture cross section of hole trap. Hole trap density at 83 K is a little higher than that at 298 K for the 850°C annealed sample. This indicates that a small number of shallow traps exist in this sample.

3.2 Electron Trap

The V_{FB} shifts due to electron injection at room temperature are shown in Fig. 3. The "turn around" effect[6),7)] is observed only for the 850°C sample at above 5×10^{18} cm^{-2} injection. This effect can be attributed to anomalous large interface trap generation. Moreover, in the case of 298 K injection, the V_{FB} shift for the 850°C sample begins to increase at a smaller electron injection number compared with the 1000 and

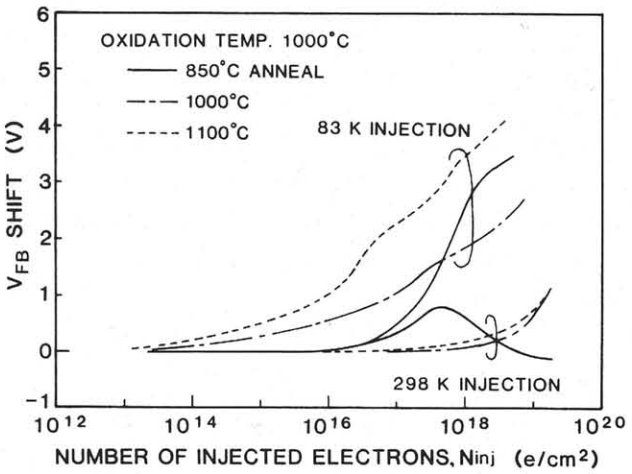

Fig.3 POA temperature dependence of flat-band voltage shifts due to electron injection

Table 2 Values of capture cross section, σ and effective density, N_{eff} for electron traps evaluated from curves shown in Fig.3

Trap	Capture Cross Section σ (cm^2)	Effective Density, Neff (cm^{-2}) 298 K Injection 850°C	298 K Injection 1000°C	298 K Injection 1100°C	83 K Injection 850°C	83 K Injection 1000°C	83 K Injection 1100°C
A	$6\sim7\times10^{-16}$	--	--	--	--	1.6×10^{11}	3.7×10^{11}
B	$4\sim8\times10^{-17}$	--	--	--	--	2.3×10^{11}	8.0×10^{11}
C	$2\sim6\times10^{-18}$	5.4×10^{11}	6.8×10^{10}	1.1×10^{11}	2.3×10^{12}	5.0×10^{11}	8.4×10^{11}
D	$1\sim2\times10^{-20}$	**	2.2×10^{12}	1.1×10^{12}	***	***	***

-- Undetected

** Undetected because of turn around effect

*** Undetected due to lack of injected carrier number at 83 K

1100°C samples. Table 2 shows results of electron trap characterization. Two traps with $\sigma=2\sim6\times10^{-18}$ and $1\sim2\times10^{-20}$ cm^2 exist in the oxide. Traps with similar cross-sections have been reported as water-related traps[8),9)]. The trap with $\sigma\cong10^{-20}$ cm^2 is not detected in the 850°C annealed sample because of the "turn around" effect. The effective density of a trap with $\sigma\cong10^{-18}$ cm^2 for the 850°C annealed sample is very large compared with that for the 1000 or 1100°C annealed samples. This result indicates that the POA temperature lowering increases water-related traps in the oxide. Under injection at 83 K, the V_{FB} shift begins to increase at low injection level and the amount of V_{FB} is larger than that for room temperature injection. Two additional electron traps with $\sigma=6\sim7\times10^{-16}$, $4\sim8\times10^{-17}$ cm^2 are detected for the 1000 and 1100°C annealed sample at 83 K, though these are not detected in the 850°C annealed sample(Table 2). These shallow traps[10)] decrease with lowering POA temperature. No "turn around" effect is observed for the 850°C sample at 83 K injection. This indicates that interface trap generation at 83 K injection is small.

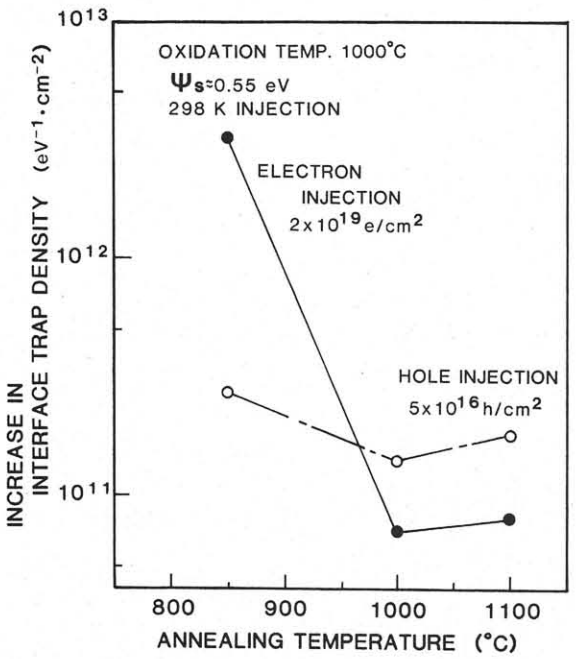

Fig.4 Increase in interface trap density due to hole and electron injection at 298 K

3.3 Interface Trap

An increase in D_{it} at the mid gap due to hole and electron injection is shown in Fig. 4. The number of generated D_{it} under hole injection is larger for the 850°C sample than for the 1000 or the 1100°C samples. The number of generated D_{it} under electron injection is also larger for the 850°C sample than for the 1000 or the 1100°C samples. The number of generated D_{it} for the 850°C sample is about 4×10^{12} $eV^{-1}\cdot cm^{-2}$ at the mid gap. This large D_{it} generation causes the "turn around" effect under electron injection.

These hot-carrier injection experiments can be summarized as follows. Low temperature (around 850°C) POA is a very effective way to decrease hole trap density in the oxide. However, it is not effective in decreasing electron traps and D_{it} generation. On the contrary, the reverse effect appears under high temperature conditions (above 1000°C) POA.

§4. Discussion

Several defect states in SiO_2 and at the $Si-SiO_2$ interface have been correlated to the electronic properties of a MOS structure. For example, hole traps correspond to oxide trivalent defect ($O{\equiv}Si\cdot$ or E' center)[11], electron traps to water related defects such as Si-OH and Si-H groups in SiO_2[12], and interface traps to trivalent Si($Si{\equiv}Si\cdot$) and to nonbridging oxygen ($Si{\equiv}Si-O\cdot$)[13]. Based on this bond defect model, we propose an OH and H diffusion model to explain the above experimental results. After the gate oxide formation and poly-Si depostion process, the oxide may contain a large number of Si-OH and Si-H bonds. These Si-OH and Si-H bonds are broken during the POA, and oxide trivalent defects which are responsible for hole traps, are generated as the following reaction.

$$O{\equiv}Si-OH \rightarrow O{\equiv}Si\cdot + OH \quad \text{or} \quad O{\equiv}Si-H \rightarrow O{\equiv}Si\cdot + H$$

During low temperature POA, Si-OH and Si-H bonds are stable and remain in SiO_2. However, the above reaction is accelerated by high temperature POA, and OH, H groups diffuse away. Therefore, many water related traps exist in SiO_2 after low temperature POA, and hole traps increase after high temperature POA. With respect to D_{it} generation, high temperature POA can increase Si-O bond strength at the interface due to densification, which leads to lower D_{it} generation under carrier injection.

§5. Summary

Low temperature POA is suitable for radiation hardened MOS devices because low hole trap density in SiO_2 can be obtained, whereas high temperature POA is a promising way to reduce hot-electron instability because of its capacity to produce low electron trap density and its small D_{it} generation. An OH or H diffusion model during high temperature annealing is proposed to explain the effect of POA on carrier trapping properties.

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References

1) T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster and H. N. Yu: IEEE Trans. Electron Devices, ED-26(1979)1430.
2) G. H. Hughes and G. J. Brucks: Solid State Tech., 22, No.7(1979)70.
3) W. R. Dawes, Jr., G. F. Derbenwick and B. L. Gregory: IEEE J. Solid-State Circuits, SC-11(1976)459.
4) E. H. Nicollian and C. N. Berglund: J. Appl. Phys., 41(1970)3052.
5) M. Khun: Solid-State Electron., 13(1970)873.
6) R. A. Gdula: J. Electrochem. Soc., 123(1976)42.
7) D. R. Young, E. A. Irene, D. J. DiMaria, R. F. Dekeersmacker and H. Z. Massond: J. Appl. Phys., 50(1979)6366.
8) E. H. Nicollian, C. N. Berglund, P. F. Schmit and J. M. Andreus, J. Appl. Phys., 42(1971)5654.
9) F. J. Feigl, D. R. Young, D. J. DiMaria, S. Lai and J. Calise: J. Appl. Phys., 52(1981)5665.
10) T. H. Ning: J. Appl. Phys., 49(1978)5997.
11) P. M. Lenahan and P. V. Dressendorfer: J. Appl. Phys., 55(1984)3495.
12) A. Hartstein and R. Young: Appl. Phys. Lett., 38(1981)631.
13) P. M. Lenahan, K. L. Brower and P. V. Dressendorfer: IEEE Trans. Nucl. Sci., NS-28(1981)4105.